

KAKATIYA INSTITUTE OF TECHNOLOGY & SCIENCE

Opp : Yerragattu Gutta, Hasanparthy (Mandal), WARANGAL - 506 015, Telangana, INDIA.

काकतीय प्रौद्योगिकी एवं विज्ञान संस्थान, वरंगल - ५०६ ०१५ तेलंगाना, भारत

కాకతీయ సాంకేతిక విజ్ఞాన శాస్త్ర విద్యాలయం, వరంగల్ - 506 001 తెలంగాణ, భారతదేశం

(An Autonomous Institute under Kakatiya University, Warangal)

(Approved by AICTE, New Delhi; Recognised by UGC under 2(f) & 12(B); Sponsored by EKASILA EDUCATION SOCIETY)

website: www.kitsw.ac.in

E-mail: principal@kitsw.ac.in

+91 9392055211, +91 7382564888

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

No: ⁵⁴³ KITS/ECED/UG-B.Tech.(ECI)/BoS-ECI (Internal)/MoM/2022

Date: 03.02.2022

Minutes of BoS-ECI Meeting

Date: 03.02.2022

Time: 4:00PM

Agenda:

1. Approval of Modifications made in Scheme & Syllabi of B. Tech. (ECI) - IV, V & VI Semester courses under URR-18, for courses with Course codes - U18CI406, U18CI504, U18CI606 & U18CI609.
2. Any other item with the permission of chair

Members Present:

Internal BoS meeting was conducted on 03.02.2022, from 4:00 pm to 4:30 pm in Digital Communication laboratory of ECE department to review & incorporate modifications in the existing Scheme & Syllabi of Courses of B. Tech. (ECI) - IV, V & VI Semester under URR-18, Courses titled U18CI406 - Microprocessors Microcontrollers, U18CI504 - Embedded System Design, U18CI606 - Artificial Intelligence and Machine Learning and U18CI609 - Embedded Networking and Applications laboratory. The following members were present during the Internal BoS meeting and offered valuable suggestions in this regard.

S. No.	Name of the Member	Designation	Position in BoS	Signature
1.	Dr. M. Raju	Assoc. Professor & HoD, ECED, KITSW	Chairperson, BoS	
2.	Dr. M. Raghu Ram	Programme Head - ECI & HoD, EIED, KITSW	Member	
3.	Prof. K. Ashoka Reddy	Senior Professor of ECED, KITSW	Member	
4.	Prof. M. Sreelatha	Senior Professor of EIED, KITSW	Member	
5.	Prof. G. Ragotham Reddy	Professor of ECED, KITSW	Member	
6.	Prof. K. Sivani	Professor of EIED, KITSW	Co-Opted Member-1	
7.	Prof. K. Venu Madhav	Professor of EIED, KITSW	Co-Opted Member-2	
8.	Dr. V. Raju	Asst. Prof. of ECED, KITSW	Co-Opted Member-3	
9.	Prof. B. Rama Devi	Professor of ECED, KITSW	Special Invitee	
10.	Sri E. Suresh	Assoc. Prof. of ECED, KITSW	Special Invitee	
11.	Sri O. Anjaneyulu	Assoc. Prof. of EIED, KITSW	Special Invitee	
12.	Dr. K. Srinivas	Asst. Prof. of EIED, KITSW	Special Invitee	

Resolutions:

1. Dr. M. Raju, HoD-ECE & Chairperson BoS-ECI welcomed all the internal members to the BoS-ECI meeting.
2. Chairperson BoS - ECI briefed the agenda points to be discussed during the meeting.
3. All the Internal members of BoS-ECI participated in the meeting and offered their valuable suggestions on:
 - (i) Modifications to be made in Scheme & Syllabi of B. Tech. (ECI) – IV, V & VI Semester courses under URR-18, for courses with Course codes – U18CI406, U18CI504, U18CI606 & U18CI609.
 - (ii) Modifications to be made in Course codes of B. Tech. (ECI) – IV & V semester courses under URR-18, for courses with Course codes – U18CI406 & U18CI504.
4. As per Internal BoS members' suggestions, the modifications were incorporated in the scheme & syllabi and the same are tabulated below:

S. No.	Course Code	Course Name	Suggestions made by the BoS members	Remarks
IV SEMESTER:				
1.	U18CI406	Microprocessors Microcontrollers	<ul style="list-style-type: none"> ▪ To change the course code (as suggested by Exam branch authorities, keeping in view of Exam automation system requirements) ▪ To change the Title & Syllabus appropriately 	Incorporated the suggested modifications in Scheme & Syllabus <u>Modification made:</u> 1. Course code of U18CI406 is changed to U18CI410 2. Course title is changed as "Microprocessor Systems and Interfacing" and the Syllabus is modified accordingly
V SEMESTER:				
3.	U18CI504	Embedded System Design	<ul style="list-style-type: none"> ▪ To change the course code (as suggested by Exam branch authorities, keeping in view of Exam automation system requirements) ▪ To change the Title & Syllabus appropriately, by giving required 	Incorporated the suggested modifications in Scheme & Syllabus <u>Modification made:</u> 1. Course code of U18CI504 is changed to U18CI509 2. Course title is

			Weightage to Microcontrollers and Embedded systems applications	changed as "Microcontrollers and Embedded Systems" and the Syllabus is modified accordingly
VI SEMESTER:				
4.	U18CI606	Artificial Intelligence and Machine Learning	▪ To change the Syllabus appropriately , by giving required Weightage to sequence of flow in course content	Incorporated the suggested modifications in Syllabus Modification made: Syllabus of U18CI606 is modified accordingly
5.	U18CI609	Embedded Networking and Applications Laboratory	▪ To change the Title & Syllabus appropriately , by giving required Weightage to IoT based sensors applications & Sensor data acquisition	Incorporated the suggested modifications in Scheme & Syllabus Modification made: Title of U18CI609 is changed as " IoT and Data Acquisition Laboratory " and the Syllabus is modified accordingly

The meeting was adjourned at 4:30pm.

Sd/-

Regards:

Dr. M. Raju

Chairperson, BoS-ECI, KITSW & Assoc. Prof. & Head, Department of ECE,
Kakatiya Institute of Technology & Science(KITSW), Yerragattu Hillock, Bheemaram,
Warangal, Telangana, India-506015.

Email: hod.ece@kitsw.ac.in



KAKATIYA INSTITUTE OF TECHNOLOGY & SCIENCE

Opp : Yerragattu Gutta, Hasanparthy (Mandal), WARANGAL - 506 015, Telangana, INDIA.

काकतीय प्रौद्योगिकी एवं विज्ञान संस्थान, वरंगल - ५०६ ०१५ तेलंगाना, भारत

(An Autonomous Institute under Kakatiya University, Warangal)

(Approved by AICTE, New Delhi; Recognised by UGC under 2(f) & 12(B); Sponsored by EKASILA EDUCATION SOCIETY)

website: www.kitsw.ac.in

E-mail: principal@kitsw.ac.in

☎ : +91 9392055211, +91 7382564888

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

Minutes of BoS-ECI Meeting

Date: 03.02.2022

Time: 4:00PM

Agenda:

1. Approval of Modifications made in Scheme & Syllabi of B. Tech. (ECI) - IV, V & VI Semester courses under URR-18, for courses with Course codes - U18CI406, U18CI504, U18CI606 & U18CI609.
2. Any other item with the permission of chair

Members Present:

Internal BoS meeting was conducted on 03.02.2022, from 4:00 pm to 4:30 pm in Digital Communication laboratory of ECE department to review & incorporate modifications in the existing Scheme & Syllabi of Courses of B. Tech. (ECI) - IV, V & VI Semester under URR-18, Courses titled U18CI406 - Microprocessors Microcontrollers, U18CI504 - Embedded System Design, U18CI606 - Artificial Intelligence and Machine Learning and U18CI609 - Embedded Networking and Applications laboratory. The following members were present during the Internal BoS meeting and offered valuable suggestions in this regard.

S. No.	Name of the Member	Designation	Position in BoS	Signature
1.	Dr. M. Raju	Assoc. Professor & HoD, ECED, KITSW	Chairperson, BoS	
2.	Dr. M. Raghu Ram	Programme Head - ECI & HoD, EIED, KITSW	Member	
3.	Prof. K. Ashoka Reddy	Senior Professor of ECED, KITSW	Member	
4.	Prof. M. Sreelatha	Senior Professor of EIED, KITSW	Member	
5.	Prof. G. Ragotham Reddy	Professor of ECED, KITSW	Member	
6.	Prof. K. Sivani	Professor of EIED, KITSW	Co-OptedMember-1	
7.	Prof. K. Venu Madhav	Professor of EIED, KITSW	Co-OptedMember-2	
8.	Dr. V. Raju	Asst. Prof. of ECED, KITSW	Co-OptedMember-3	
9.	Prof. B. Rama Devi	Professor of ECED, KITSW	Special Invitee	
10.	Sri E. Suresh	Assoc. Prof. of ECED, KITSW	Special Invitee	
11.	Sri O. Anjaneyulu	Assoc. Prof. of EIED, KITSW	Special Invitee	
12.	Dr. K. Srinivas	Asst. Prof. of EIED, KITSW	Special Invitee	

Resolutions:

1. Dr. M. Raju, HoD-ECE & Chairperson BoS-ECI welcomed all the internal members to the BoS-ECI meeting.
2. Chairperson BoS - ECI briefed the agenda points to be discussed during the meeting.
3. All the Internal members of BoS-ECI participated in the meeting and offered their valuable suggestions on:
 - (i) Modifications to be made in Scheme & Syllabi of B. Tech. (ECI) – IV, V & VI Semester courses under URR-18, for courses with Course codes – U18CI406, U18CI504 & U18CI609.
4. As per Internal BoS members' suggestions, the modifications were incorporated in the scheme & syllabi and the same are tabulated below:

S. No.	Course Code	Course Name	Suggestions made by the BoS members	Remarks
IV SEMESTER:				
1.	U18CI406	Microprocessors Microcontrollers	Change the Title & Syllabus appropriately	Incorporated the suggested modifications in Scheme & Syllabus Modification made: Title of U18CI406 is changed as "Microprocessor Systems and Interfacing" and Syllabus modified accordingly
V SEMESTER:				
2.	U18CI504	Embedded System Design	Change the Title & Syllabus appropriately, by giving required Weightage to Microcontrollers and Embedded systems applications	Incorporated the suggested modifications in Scheme & Syllabus Modification made: Title of U18CI504 is changed as "Microcontrollers and Embedded Systems" and Syllabus modified accordingly
VI SEMESTER:				
3.	U18CI606	Artificial Intelligence and Machine Learning	Change the Syllabus appropriately, by giving required Weightage to sequence of flow in course content	Incorporated the suggested modifications Syllabus Modification made: Syllabus modified

				accordingly
4.	U18CI609	Embedded Networking and Applications Laboratory	Change the Title & Syllabus appropriately, by giving required Weightage to IoT based sensors applications & Sensor data acquisition	Incorporated the suggested modifications in Scheme & Syllabus <u>Modification made:</u> Title of U18CI609 is changed as "IoT and Data Acquisition Laboratory" and Syllabus modified accordingly

The meeting was adjourned at 4:30pm.

Sd/-

Regards:

Dr. M. Raju

Chairperson, BoS-ECI, KITSW & Assoc. Prof. & Head, Department of ECE, Kakatiya Institute of Technology & Science(KITSW), Yerragattu Hillock, Bheemaram, Warangal, Telangana, India-506015.

Email: hod.ece@kitsw.ac.in

U18CI406 MICROPROCESSOR SYSTEMS AND INTERFACING

Class: B.Tech. IV-Semester

Branch: Electronics Communication & Instrumentation Engg. (ECI)

Teaching Scheme:

L	T	P	C
3	-	-	3

Examination Scheme:

Continuous Internal Evaluation	40 marks
End Semester Examination	60 marks

Course Learning Objectives(LOs):

This course will develop students' knowledge on /in...

LO1: architectural features of 8086 microprocessor

LO2: programming concepts of 8086 microprocessor

LO3: interfacing of peripheral devices to 8086 through 8255 (PPI), 8257 (DMA), 8259 (PIC)

LO4: serial data communication types and RS232 & IEEE 488 bus standards

UNIT-I (9)

Introduction to Microprocessors - Evolution, Overview of 8085 MPU architecture

8086 Family Architecture: Organization of 8086 CPU, Concept of memory segmentation, Segment registers, Physical and Logical addressing, Addressing modes, Instruction formats, Instruction set

UNIT-II (9)

Assembly Language Programming: Assembler directives, Simple programming of 8086, Arithmetic, Logical and Data processing programs; Implementation of control loops, Structures, Strings, Procedures, Macros

Pin configuration, Minimum / Maximum modes, Timing diagrams, Delay subroutines

UNIT-III (9)

Interfacing with 8086: 8086 Interrupts, Interrupt service routines, Priority interrupt controller 8259, Programmable peripheral interface 8255, Interfacing of switches, Keyboards, LEDs, Stepper motor, ADCs and DACs

UNIT-IV (9)

DMA Controller 8257, Programmable Timer/Counter 8254

Serial Data Communication through 8086: Types of serial communication, Synchronous and Asynchronous communication, Serial data communication through USART 8251, Serial data communication standards, RS-232, IEEE 488 Bus (GPIB)

[Signature]

(Member, BOS-ECI)

[Signature]

[Signature]

[Signature]

[Signature]

[Signature]

[Signature]

[Signature]

[Signature]

[Signature]

Text Books:

- [1] D.V.Hall, *Microprocessors and Interfacing: Programming & Hardware*, 2nd ed. New Delhi: Tata McGraw Hill, 1992. (Chapters 3 to 10)
- [2] Yuchang Liu and Glen A. Gibson, *Microcomputer Systems - The 8086/8088 Family Architecture, Programming and Design*, 2nd ed. New Delhi: PHI, 1995. (Chapters 2 to 11)

Reference Books:

- [1] Ramesh Gaonkar, *Microprocessor Architecture, Programming and Applications with the 8085*, 6th ed. Mumbai: Penram International Publishing (I) Pvt. Ltd., 2013.
- [2] Kenneth J. Ayala, *Ayala Kenneth, The 8086 Microprocessor: Programming and Interfacing the PC*, Minnesota: West Publishing Company, 1994.
- [3] Barry B. Brey, *The Intel Microprocessors: Architecture, Programming and Interfacing*, 2nd ed. New Delhi: PHI, 1998.

Course Learning Outcomes(COs):

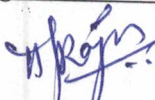
On completion of this course, students will be able to...


- CO1: discuss architectural and programming features of 8086
CO2: develop assembly language programs (ALPs) to solve data processing problems
CO3: design hardware circuits for interfacing of i/o devices with 8086 μ p through PPI / PIC
CO4: utilize serial communication standards USART&RS232 and IEEE 488 bus standards for data transfer

Course Articulation Matrix (CAM):U18CI406 MICROPROCESSOR SYSTEMS AND INTERFACING

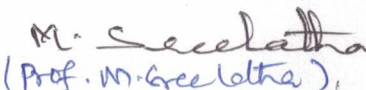

CO	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PO 12	PSO 1	PSO 2
CO1 U18CI406.1	1	1	1	-	-	-	-	-	-	-	-	2	2	2
CO2 U18CI406.2	1	2	2	-	1	-	-	-	-	-	-	2	2	2
CO3 U18CI406.3	1	2	2	-	1	-	-	-	-	-	-	2	2	2
CO4 U18CI406.4	1	2	2	-	-	-	-	-	-	-	-	2	2	2
U18CI406	1	1.75	1.75	-	1	-	-	-	-	-	-	2	2	2


Signatures of Internal BOS Members:

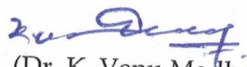

(Dr. M. Raju)
Chairperson, BoS, ECI



(Dr. M. Raghuram)
Member, BoS, ECI



(Dr. K. Ashoka Reddy)
Member, BoS, ECI



(Prof. M. G. Sathya),
member, BoS, ECI

(Dr. G. Raghobham Reddy)
Member, BoS, ECI

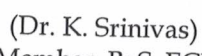

(Dr. K. Sivani)
Member, BoS, ECI



(Dr. K. Venu Madhav)
Member, BoS, ECI


(Dr. V. Raju)
Member, BoS, ECI


(Prof. B. Rama Devi)
Member, BoS, ECI


(Sri E. Suresh)
Member, BoS, ECI


(Dr. K. Srinivas)
Member, BoS, ECI


(Dr. K. Srinivas)
Member, BoS, ECI

U18CI504 MICROCONTROLLERS AND EMBEDDED SYSTEMS

Class: B.Tech. VI – Semester

Branch: Electronics Communication & Instrumentation Engineering (ECI)

Teaching Scheme:

L	T	P	C
3	-	-	3

Examination Scheme:

Continuous Internal Evaluation	40 marks
End Semester Examination	60 marks

Course Learning Objectives (LOs):

This course will develop students' knowledge on / in...

LO1: architecture, interrupts and addressing modes of 8051

LO2: hardware and software for interfacing keyboards, display and data converters with 8051

LO3: the issues related to overall design issues related to hardware and software of an embedded system and programming in "Embedded C"

LO4: basic functions of OS, multiprocessing and multitasking, task scheduling, synchronization and choosing the proper RTOS for an embedded system development

UNIT-I (9)

Overview of 8051 Microcontroller, 8051 Architecture, Hardware units of 8051, Memory organization, I/O ports, Timers and counters, Serial data input and output, Interrupts of 8051, 8051 Assembly language programming concepts, Addressing modes

UNIT - II (9)

Programming model, Instruction set of 8051 and programming, Microcontroller interfacing with keyboard & display Units (LED and LCD), Interfacing of DAC and ADC, Serial data communication, Use of interrupts & service routines

UNIT - III (9)

Embedded System: Introduction, Characteristics and components of an embedded system, Fundamental issues in hardware software co-design, Embedded firmware design approaches

Programming in "Embedded C": C vs Embedded C, Data types and storage classes, Arrays, pointers & I/O operations, Structures & bit fields, Volatile qualifier, Coding interrupt service routines, Reentrant and recursive functions

UNIT - IV (9)

Real-Time Operating System (RTOS) based Embedded System Design: Operating system basics, Types of operating systems, Tasks, Process & threads, Multiprocessing and multitasking, Task scheduling, Task communication, Task synchronization, Device drivers, Selection of RTOS

Text Books:

- [1] Shibu K V, *Introduction to Embedded Systems*, New Delhi: McGraw Hill Education (India) Pvt. Ltd., 2009. (Chapter 1, 2, 5, 6, 7, 9 and 10)
- [2] Manish K Patel, *The 8051 Microcontroller Based Embedded Systems*, New Delhi: McGraw Hill Education (India) Pvt. Ltd., 2014. (Chapter 2 to 21)

[Signature]

(member, RRS-ECI)

[Signature]

[Signature]
M. Sreedhar

[Signature]

[Signature]

[Signature]

[Signature]

[Signature]

[Signature]

Reference Books:

- [1] Kenneth J. Ayala, *The 8051 Microcontroller*, 3rd ed. Noida: Cengage learning, 2007.
- [2] Md. Ali Mazidi, Janice G Mazidi and Rolin D. McKinlay, *The 8051 Microcontroller and Embedded Systems Using Assembly and C*, 2nd ed. New Delhi: Pearson Education India, 2011.
- [3] Sriram V. Iyer & Pankaj Gupta, *Embedded Real Time Systems Programming*, New Delhi: TMH, 2003.

Course Learning Outcomes (COs):

On completion of this course, students will be able to...

CO1: discuss the architectural features, viz. memory organization, interrupts and addressing modes of 8051

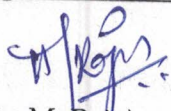
CO2: design required hardware interface and implement required software for interfacing keyboards, display units and data converters with 8051


CO3: develop embedded firmware using Embedded C for embedded applications


CO4: discuss about fundamental issues in task scheduling, communication and synchronization in an RTOS

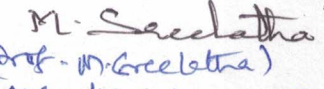
Course Articulation Matrix (CAM): U18CI504 MICROCONTROLLERS AND EMBEDDED SYSTEMS															
CO		PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PO 12	PSO 1	PSO 2
CO1	U18CI504.1	1	1	2	1	2	-	-	-	-	-	-	2	2	2
CO2	U18CI504.2	1	1	2	1	2	-	-	-	-	-	-	2	2	2
CO3	U18CI504.3	1	1	2	1	2	-	-	-	-	-	-	2	2	2
CO4	U18CI504.4	1	1	2	1	2	-	-	-	-	-	-	2	2	2
U18CI504		1	1	2	1	2	-	-	-	-	-	-	2	2	2

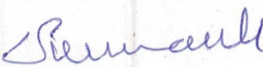
Signatures of Internal BOS Members:



(Dr. M. Raju)
Chairperson, BoS, ECI



(Dr. M. Raghuram)
Member, BoS, ECI

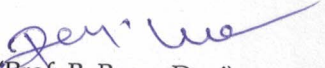

(Dr. K. Ashoka Reddy)
Member, BoS, ECI

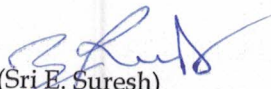

(Dr. G. Raghotham Reddy)
Member, BoS, ECI

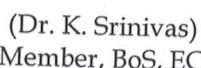

(Dr. K. Sivani)
Member, BoS, ECI



(Dr. K. Venu Madhav)
Member, BoS, ECI


(Dr. V. Raju)
Member, BoS, ECI


(Prof. B. Rama Devi)
Member, BoS, ECI


(Sri E. Suresh)
Member, BoS, ECI


(Dr. K. Srinivas)
Member, BoS, ECI


(Dr. K. Srinivas)
Member, BoS, ECI

U18CI606 ARTIFICIAL INTELLIGENCE AND MACHINE LEARNING

Class: B.Tech.VI-Semester

Branch: Electronics Communication and Instrumentation (ECI)

Teaching Scheme:

Examination Scheme:

L	T	P	C
3	-	-	3

Continuous Internal Evaluation	40 marks
End Semester Examination	60 marks

Course Learning Objectives (LOs):

This course will develop students' knowledge on /in...

LO1: fundamentals of AI, problem solving, search methods and applications of expert system

LO2: artificial neural network based algorithms and its analysis for data types

LO3: standard concepts, supervised & unsupervised machine learning algorithms for classification

LO4: applications of machine learning in fields of image processing, biomedical signal processing & speech processing

UNIT-I (9)

Artificial Intelligence (AI): Introduction, fundamentals of artificial intelligence, history of artificial intelligence, state of the art, intelligent agents, agents and environments, concept of rationality, nature of environments, structure of agents, solving problems by searching, problem-solving agents, example problems, searching for solutions, uninformed search strategies, informed (heuristic) search strategies, heuristic functions

UNIT - II (9)

Artificial Neural Networks: Biological neuron structure, artificial neuron, implementations of boolean functions using Mc Pitts neuron, gradient based learning, hidden units, architecture design, back propagation algorithm, Convolution Neural Networks (CNN) - Introduction, data types, efficient convolution algorithm, activation functions, Recurrent Neural Networks (RNN), Deep Recurrent Neural Networks (DRNN), Long Short Term Memory (LSTM)

UNIT-III(9)

Machine Learning (ML): Introduction to ML, types of learning, applications of ML

Supervised learning: Linear regression, polynomial regression, classification methods- KNN classifier, decision trees, naïve bayes, support vector machines, logistic regression analysis

Unsupervised Learning: Clustering - K-means clustering, hierarchical clustering; dimensionality reduction - PCA (principal component analysis), Fischer's discriminant analysis, ensemble learning - boosting & bagging approaches

UNIT - IV(9)

Machine learning in Image processing: Fundamentals of image processing, feature mapping case study on image classification using artificial neural networks

Machine learning in biomedical signal processing: Fundamentals of biomedical signals, feature extraction from database of biomedical signals (ECG/EMG), case study on biomedical signal classification.

Introduction to Speech Processing: Process of speech production a block diagram approach, Classification of speech sounds, speech recognition using HMM

[KITSW-Syllabi for III-VI Semester B.Tech. (ECI) 4-year Degree Programme]

Signature
M. Saeelatha

Signature
(member - B.Tech. ECI)

Text Books:

- [1]. Russell, S. & Norvig, *Artificial Intelligence: A Modern Approach*, 4th ed. New York: Pearson Education Publications, 2010. (Chapters: 1 to 11)
- [2]. Giuseppe Bonaccorso, *Machine Learning Algorithms*, 2nd Edition, Packt, 2018, (Chapters 1,2,3,4,,5,6,7,8,9,10,11,13,15)

Reference Books:

- [1]. U Dinesh Kumar and Manaranjan Pradhan, *Machine Learning using Python*, New Delhi: John Wiley & sons, 2019. (Chapters 1,2,3,4,5,,6,7,8,9,10)
- [2]. Himanshu Singh, *Practical machine learning and image processing*, Apress, India, 2019 (chapters: 5, 6)
- [3]. Abdulhamit Subasi, *Practical guide for biomedical signal analysis using machine learning techniques*, Academic press, UK, 2019. (chapters: 2,3,4)
- [4]. Andreas C. Mueller and Sarah Guido, *Introduction to Machine Learning with Python*, Sebastopol, CA: O'Reilly Media, 2016.
- [5]. Vinod Chandra S. S, Anand Hareendran S, *Artificial Intelligence and Machine Learning*, Prentice Hall, India, 2014.
- [6]. Ethem Alpaydin, *Introduction to machine learning*, 2nd ed. Cambridge: MIT Press, USA, 2010.
- [7]. Denis Rothman, *Artificial Intelligence by Example*, 2nd ed. Birmingham: Packt Publishing, 2020.

Course Research Papers: Research papers (Journal/Conference papers) relevant to the course content will be posted by the course faculty in Course Web page

Course Patents: Patents relevant to the course content will be posted by the course faculty in Course Web page

Course Projects: Course project is an independent project carried out by the student during the course period, under the supervision of course faculty. Course faculty will post few course projects titles in Course Web page. Students are encouraged to come up and experiment with the ideas that interest them.

Course Learning Outcomes (COs):

On completion of this course, students will be able to...

CO1: select a suitable AI based intelligent system and solution for problem solving

CO2: estimate different AI algorithms like CNN, RNN, DRNN and LSTM

CO3: analyze supervised & unsupervised learning methods for classification of data

CO4: analyze the machine learning applications in the areas of signal, image & speech processing

Course Articulation Matrix (CAM) U18CI606 ARTIFICIAL INTELLIGENCE AND MACHINE LEARNING

CO		PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PO 12	PSO 1	PSO 2
CO1	U18CI606.1	2	1	1	1	-	-	-	1	1	1	-	1	2	1
CO2	U18CI606.2	2	2	1	1	1	-	-	1	1	1	-	1	2	1
CO3	U18CI606.3	2	2	1	1	1	-	-	1	1	1	-	1	2	1
CO4	U18CI606.4	2	2	1	1	1	-	-	1	1	1	-	1	2	1
U18EC606		2	1.5	2	1.75	1.75	1	-	1	1	1	-	1	2	2

U18CI609 IoT AND DATA ACQUISITION LABORATORY

Class: B.Tech. VI-Semester

Branch: Electronics Communication & Instrumentation Engineering

Teaching Scheme:

L	T	P	C		
-	-	2	1	Continuous Internal Evaluation:	60 marks
				End Semester Exam:	40 marks

Examination Scheme:

Course Learning Objectives (LOs):

This course will develop students' knowledge in/on...

LO1: interfacing sensors to Raspberry Pi 3 using Python

LO2: visualize the sensor data using cloud service

LO3: measure and analyze the sensors characteristics using LabVIEW

LO4: building cloud-based dashboard for IoT applications using LabVIEW

List of Experiments

The following experiments are to be performed on Raspberry Pi 3 board by developing Python programs.

1. Reading Temperature and Humidity values into Raspberry Pi
2. Controlling a servo motor with Raspberry Pi
3. Visualizing Temperature and Humidity data on ThingSpeak cloud
4. Cloud based implementation of IoT using a MQTT Broker
5. Triggering an IFTTT applet from Raspberry Pi
6. Controlling LED brightness with IFTTT Applet using dweet.io service
7. Basic Programming in LabVIEW
8. Advance features in LabVIEW
9. Reading and writing an analog signal using NI-DAQ device
10. Recording an analog signal acquired in a spreadsheet
11. Triggering an alarm with temperature data from NI - myDaq
12. Measuring Acceleration and Gyroscope data using NI - myRio
13. Data communication with TCP/IP Using LabVIEW
14. Communicating with Google Firebase cloud using LabVIEW

Laboratory Manual:










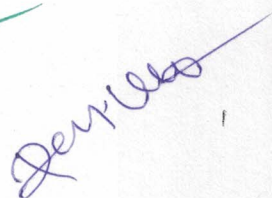
- [1] Internet of Things Laboratory Manual, Dept. of ECE, KITSW.

Reference Book

- [1] Colin Dow, Internet of Things Programming Projects, Birmingham: Packt Publishing, 2018.

[Handwritten signatures and notes at the bottom of the page]

Course Articulation Matrix: U18CI609 IoT & DAQ Lab															
CO		PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PO 12	PSO 1	PSO 2
CO1	U18CI609.1	2	2	2	1	1	-	1	1	1	1	-	1	2	1
CO2	U18CI609.2	2	2	2	1	1	-	1	1	1	1	-	1	2	1
CO3	U18CI609.3	2	2	2	1	2	-	1	1	1	1	-	1	2	1
CO4	U18CI609.4	2	2	2	1	2	-	1	1	1	1	-	1	2	1
U18CI609		2	2	2	1	1.5	-	1	1	1	1	-	1	2	1



ORDERS

Sub: KITS, Warangal - UGC Autonomous status - Constitution of Board of Studies (BoS) for Electronics & Communication Engineering (ECE) Course - Modified Orders - Issued.

- Ref : 1. Letter No. F.22-1/2-14(AC), Dt. 19.6.2014 from the Joint Secretary, UGC, New Delhi.
2. Letter No. 350/CDC/KU/2014, Dt. 18.8.2014. from the Registrar, Kakatiya University, Warangal.
3. This office Order No. KITS/Acad/2014, Date: 20-8-2014.
4. Note No. 1113/ECE/KITS/2016, Date : 02-09-2016 from HOD, ECE

In continuation of the order cited 3 above, the Board of Studies (BoS) for Electronics & Communication Engineering (ECE) Course has been constituted with the following members for a period of two (2) years with effect from the date of issue of these orders.

- | | |
|---|---|
| 1. Prof. G. Raghotham Reddy
Prof. & HoD of ECE, KITSW | --- Chairperson, BoS of ECE |
| 2. Prof. K. Ashoka Reddy
Prof. of ECE, KITSW | --- Member |
| 3. Smt. S.P. Girija
Assoc. Prof. of ECE, KITSW | --- Member |
| 4. Sri E. Suresh
Assoc. Prof. of ECE, KITSW | --- Member |
| 5. Dr. B. Rama Devi
Assoc. Prof. of ECE, KITSW | --- Member |
| 6. Dr. P. Chandra Sekhar
Professor, Dept. of ECE
University College of Engineering,
Osmania University, Hyderabad. | --- External Member |
| 7. Dr. N. V. S. N. Sarma
Professor, Dept. of ECE,
NIT, Warangal. | --- External Member |
| 8. University Nominee | --- External Member |
| 9. Sri Praveen Jambholkar
Technical Director,
Cybermotion Technologies Pvt. Ltd,
Hyderabad. | --- External Member
(from Industry) |
| 10. Sri Prabhod Kumar Enumula
Co-founder & Director
Iween Software Solutions, Bangalore. | -- External Member
(Post Graduate Meritorious Alumnus) |
| 11. Smt. A. Vijaya
Assoc. Prof. of ECE, KITSW | --- Co-Opted Member |

The Board shall exercise such powers, perform such duties and functions in accordance with the procedure laid down in UGC norms for the Kakatiya Institute of Technology & Science, Warangal.

The meeting of the Board shall ordinarily be convened as and when necessary, at least once in a year.

However, any member of the Board of Studies shall cease to be a member when he vacates the office, which he was holding at the time of his/her appointment, unless otherwise permitted by the authority.


PRINCIPAL

To
The Persons concerned

Copy to: 1. Secretary & Correspondent

2. Treasurer

3. Director

4. All Deans

5. All Heads of Departments

6. Academic Section

KAKATIYA INSTITUTE OF TECHNOLOGY & SCIENCE, WARANGAL-15
(An Autonomous Institute under Kakatiya University, Warangal)
DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

No. 77/ECE/KITS/2020

Date: 14.02.2020

Submitted to the Principal:

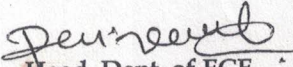
Sub: Nomination of **Internal members, External members (from Industry) and External member (Post Graduate Meritorious Alumnus – Industry/Academia) - Constitution of Board of Studies (BoS) for B.Tech. Electronics & Communication Engineering (ECE) Programme – Reg.**

Ref : 1. Office Order No. KITS/Acad/Autonomous-BoS (ECE)/2018, Date: 12.5.2018

Ref: 2. No. KITS/Acad/Autonomous-BoS (ECE)/2020, dated on 31.01.2020

With reference to the above cited letter the following members nominated for the department Board of Studies (BoS) of B.Tech. ECE Department, KITS, Warangal.

S. No.	Name of the Member	Designation	Position in BoS
1.	Dr. B. Rama Devi	HoD ECE, KITSW	Chairperson, BoS
2.	Dr. K. Ashoka Reddy	Senior Professor of ECE Dept. KITSW	Member
3.	Dr. G. Raghotham Reddy	Professor of ECE Dept. KITSW	Member
4.	S. P. Girija	Assoc. Prof. of ECE Dept. KITSW	Member
5.	E. Suresh	Assoc. Prof. of ECE Dept. KITSW	Member
6.	Surya Kanth V Gangasetty	Professor, IIIT, Hyderabad,	External Member (from renowned Academic Institute)
7.	Dr.L.Anjaneyulu	Professor & Head, Dept. of ECE, NIT, Warangal	External Member (from renowned Academic Institute)
8.	Prof. T. Srinivasulu	Professor, Dept. of ECE, KUCE, KU Dean, Faculty of Engineering, KU, Warangal	External Member (University Nominee)
9.	S.Venkateshwar Rao	AMD India Pvt.Ltd. Hyderabad, HITEC City, Madhapur, Hyderabad, Telangana	External Member (from Industry)
10.	Dr. Vijender Basi Reddy	Scientist, ISRO, Hyderabad.	External Member (from Industry)
11.	Dr. G Sanath Kumar,	Deputy Director, Central Institute of Tool Design (CITD), Hyderabad	External Member (from Industry)
12.	V.Madhan Kumar	Lead Designer, Synopsys, Kondapur, Kothaguda, Hyderabad, Telangana (M.Tech 2009-11)	External Member (Post Graduate Meritorious Alumnus – Academia/Industry)
13.	A.Vijaya	Assoc. Prof. of ECE Dept. KITSW	Co-Opted Member-1
14.	Dr. M. Raju	Assoc. Prof. of ECE Dept. KITSW	Co-Opted Member-2
15.	Dr. V.Venkateshwar Reddy	Assoc. Prof. of ECE Dept. KITSW	Co-Opted Member-3


Head, Dept. of ECE

KAKATIYA INSTITUTE OF TECHNOLOGY & SCIENCE, WARANGAL-15
OFFICE OF THE PRINCIPAL



No. 80/OP/KITS/2020

Date: 03/02/2020

Note to all Heads of the Departments:

Sub: Constitution of revised Board of Studies (BoS) - Reg.

- Ref: 1. Academic section note dated 31.1.2020 - constitution of BoS for programmes offered by departments
2. This office note No. 75/OP/KITS/2020, dated 31.1.2020 - Guidelines for nominating experts on BoS

In partial modification to the academic section note dated 31.01.2020, vide reference (1) cited, the HoDs are requested to **constitute a completely revised Board of Studies (BoS)** for the programmes offered by their departments.

In revising the BoS, HoDs are advised to retain the University Nominee at Sl. No.8 of BoS structure.

The HoDs are further requested to follow the guidelines stipulated for nominating the experts under Industry and Academia categories vide reference (2) cited.

The HoDs can take help from the Principal's office, in case of any requirement for sending letter to the experts officially through the Principal.


PRINCIPAL

Copy to: 1. Secretary & Correspondent
2. All Deans



KAKATIYA INSTITUTE OF TECHNOLOGY & SCIENCE, WARANGAL-15
(An Autonomous Institute under Kakatiya University, Warangal)

No.KITS/Acad/Autonomous-BoS (ECE)/2018

Date: 12.5.2018

ORDERS

Sub: KITS, Warangal – UGC Autonomous status - Constitution of Board of Studies (BoS) for Electronics & Communication Engineering (ECE) Course – Modified Orders - Issued.

Ref : 1. Letter No. F.22-1/2-14(AC), Dt. 19.6.2014 from the Joint Secretary, UGC, New Delhi.

2. Letter No. 350/CDC/KU/2014, Dt. 18.8.2014. from the Registrar, Kakatiya University, Warangal.

3. This office Order No. KITS/Acad/2014, Date: 20-8-2014.

4. Note No. 1113/ECE/KITS/2016, Date : 02-09-2016 from HOD, ECE

5. This office Order No.KITS/Acad/Autonomous-BoS(ECE)/2016, Date: 3.10.2016.

In continuation of the order cited 5 above, the Board of Studies (BoS) for Electronics & Communication Engineering (ECE) Course has been constituted with the following members for a period of two (2) years with effect from the date of issue of these orders.

- | | | |
|---|-----|---|
| 1. Dr. G. Raghotham Reddy
Prof. & Head, Dept. of ECE,
KITS, Warangal | --- | Chairperson, BoS in ECE |
| 2. Dr. K. Ashoka Reddy
Prof. of ECE,
KITS, Warangal | --- | Member |
| 3. Smt. S.P. Girija
Assoc. Prof. of ECE,
KITS, Warangal | --- | Member |
| 4. Sri E. Suresh
Assoc. Prof. of ECE,
KITS, Warangal | --- | Member |
| 5. Dr. B. Rama Devi
Assoc. Prof. of ECE,
KITS, Warangal | --- | Member |
| 6. Dr. P. Chandra Sekhar
Professor & Head, Dept. of ECE,
University College of Engineering,
Osmania University, Hyderabad. | --- | External Member |
| 7. Dr. N. V. S. N. Sarma
Professor, Dept. of ECE,
NIT, Warangal. | --- | External Member |
| 8. Prof. T. Srinivasulu
Professor, Dept. of ECE, KUCE, KU
Dean, Faculty of Engineering
Kakatiya University, Warangal | --- | External Member
(University Nominee) |
| 9. Sri Praveen Jambholkar
Technical Director,
Cybermotion Technologies Pvt. Ltd,
Hyderabad. | --- | External Member
(from Industry) |

P.T.O



KAKATIYA INSTITUTE OF TECHNOLOGY & SCIENCE

Opp : Yerragattu Gutta, Hasanparthy (Mandal), WARANGAL - 506 015, Telangana, INDIA.

काकतीय प्रौद्योगिकी एवं विज्ञान संस्थान, वरंगल - ५०६ ०१५ तेलंगाना, भारत

కాకతీయ సాంకేతిక విజ్ఞాన శాస్త్ర విద్యాలయం, వరంగల్ - ౫౦౬ ౦౧౫ తెలంగాణ, భారతదేశము

(An Autonomous Institute under Kakatiya University, Warangal)

(Approved by AICTE, New Delhi; Recognised by UGC under 2(f) & 12(B); Sponsored by EKASILA EDUCATION SOCIETY)

Est'd-1980
KITSW

website: www.kitsw.ac.in

E-mail: principal@kitsw.ac.in

☎ : +91 9392055211, +91 7382564888

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

Minutes of BoS-ECE Meeting

Date: 05.02.2022

Time: 12:00PM

Agenda:


1. Approval of Modifications made in Syllabi of B. Tech. (ECE) - V & VI Semester and M.Tech. (CESP) - II Semester courses under URR-18 & PRR-20, for courses with Course codes - U18EC503, U18EC605, U18EC606 & P20SP201.
2. Any other item with the permission of chair

Members Present:

Internal BoS meeting was conducted on 05.02.2022, from 12:00 pm to 12:45 pm in Digital Communication laboratory of ECE department to review & incorporate modifications in the existing Syllabi of Courses of B. Tech. (ECE) -V & VI Semester under URR-18 and M.Tech. (CESP) - II Semester under PRR-20, Courses titled U18EC503 - Communication Systems, U18EC605 - VLSI Circuits and Systems, U18EC606 - Embedded Systems with ARM Processor and Application and P20SP201 - Software Defined Radio.

The following members were present during the Internal BoS meeting and offered valuable suggestions in this regard.

S. No.	Name of the Member	Designation	Position in BoS	Signature
1.	Dr. M. Raju	HoD ECE, KITSW	Chairperson, BoS	
2.	Dr. K. Ashoka Reddy	Senior Professor of ECE Dept. KITSW	Member	
3.	Dr. G. Raghotham Reddy	Professor of ECE Dept. KITSW	Member	
4.	Dr. B. Rama Devi	Professor of ECE Dept. KITSW	Member	
5.	Smt. S. P. Girija	Assoc. Prof. of ECE Dept. KITSW	Member	
6.	Sri. E. Suresh	Assoc. Prof. of ECE Dept. KITSW	Member	
7.	Smt. A. Vijaya	Assoc. Prof. of ECE Dept. KITSW	Co-Opted Member-1	
8.	Dr. V. Venkateshwar Reddy	Assoc. Prof. of ECE Dept. KITSW	Co-Opted Member-2	
9.	Dr. K. Ramudu	Asst. Prof of ECE Dept, KITSW	Special Invitee	
10.	Sri. D.Venu	Asst. Prof of ECE Dept, KITSW	Special Invitee	
11.	Sri. R. Srikanth	Asst. Prof of ECE Dept.	Special Invitee	

		KITSW		
12.	Sri. P. Chiranjeevi	Asst. Prof of ECE Dept, KITSW	Special Invitee	

Resolutions:

1. Dr. M. Raju, HoD-ECE & Chairperson BoS-ECE welcomed all the internal members to the BoS-ECE meeting.
2. Chairperson BoS - ECE briefed the agenda points to be discussed during the meeting.
3. All the Internal members of BoS-ECE participated in the meeting and offered their valuable suggestions on:
 - (i) Modifications to be made in Scheme & Syllabi of B. Tech. (ECE) - V & VI Semester and M.Tech. (CESP) - II Semester courses under URR-18 & PRR-20, for courses with Course codes - U18EC503, U18EC605, U18EC606 & P20SP201.
4. As per Internal BoS members' suggestions, the modifications were incorporated in the scheme & syllabi and the same are tabulated below:

S. No.	Course Code	Course Name	Suggestions made by the BoS members	Remarks
B.Tech. (ECE) V SEMESTER:				
1.	U18EC503	Communication Systems	Change the Syllabus appropriately, by giving required Weightage to analog and digital communications	Incorporated the suggested modifications in Syllabus Modification made: Syllabus modified accordingly
B.Tech. (ECE) VI SEMESTER:				
2.	U18EC605	VLSI Circuits and Systems	Change the Syllabus appropriately, by giving required Weightage to sequence of flow in course content	Incorporated the suggested modifications Syllabus Modification made: Syllabus modified accordingly
3.	U18EC606	Embedded Systems with ARM processor and Applications	Change the Syllabus appropriately, by giving required Weightage to sequence of flow in course content	Incorporated the suggested modifications Syllabus Modification made: Syllabus modified accordingly
M.Tech. (CESP) II-Semester:				
4.	P20SP201	Software Defined Radio	Change the Syllabus appropriately, by giving required Weightage to sequence of flow in course	Incorporated the suggested modifications Syllabus

			content	Modification made: Syllabus modified accordingly
--	--	--	---------	---

The meeting was adjourned at 12:45pm.

Regards:

Dr. M. Raju

*Chairperson, BoS-ECE, KITSW & Assoc. Prof. & Head, Department of ECE,
Kakatiya Institute of Technology & Science(KITSW), Yerragattu Hillock, Bheemaram,
Warangal, Telangana, India-506015.*

Email: hod.ece@kitsw.ac.in

U18EC503 COMMUNICATION SYSTEMS

Class: B.Tech. V – Semester

Branch: Electronics and Communication Engineering(ECE)

Teaching Scheme:

L	T	P	C
3	-	-	3

Examination Scheme:

Continuous Internal Evaluation	40 marks
End Semester Examination	60 marks

Course Learning Objectives (LOs):

This course will develop students' knowledge on /in...

LO1: linear modulation strategies that constitute the amplitude modulation

LO2: angle modulation & pulse modulation

LO3: source coding, digital modulation techniques & baseband data transmission systems

LO4: bandpass data transmission systems & channel coding techniques

UNIT-I (9)

Amplitude Modulation: Introduction, Elements of Communication System, Amplitude Modulation, Double Sideband-Suppressed Carrier Modulation, Costas Receiver, Single-Sideband Modulation, Vestigial Sideband Modulation, Noise in Communication Systems- Sources of Noise-Shot noise, White noise, Band-Pass Receiver Structures-Super Heterodyne Receiver-Intermediate frequency-AGC, Noise in AM, Noise in DSB-SC, Noise in SSB-SC.

UNIT-II (9)

Angle Modulation: Basic Definitions-Frequency Modulation-Phase Modulation, Relationship between PM and FM Waves, Narrow-Band Frequency Modulation, Wide-Band Frequency Modulation, Transmission Bandwidth of FM Waves, Generation of FM Waves, Demodulation of FM Signals-Phase discriminator, Phase Locked Loop, Noise in FM, Pre-emphasis and De-emphasis.

Pulse Modulation: Transition from Analog to Digital Communications, Sampling Process, Pulse-Amplitude Modulation, Pulse-Position Modulation.

UNIT-III (9)

Digital Modulation: Elements of Digital communication system, Source coding, Discrete Memoryless Source (DMS), Measure of Information, Entropy, Information Rate, Source coding-Shannon Fano, Huffman Coding, Gaussian Channel capacity – Shannon bound, Pulse-Code Modulation (PCM), Quantization, Quantization error, Signal to quantization noise ratio, Delta modulation (DM), Adaptive Delta Modulation (ADM), Comparison of PCM and DM

Baseband Data Transmission(Introduction): Inter Symbol Interference, Pulse shaping, Eye Pattern, Equalization

UNIT - IV (9)

Band-pass Data Transmission: Coherent Binary Phase Shift Keying (BPSK), Differential Phase Shift Keying (DPSK), Coherent Binary Frequency shift keying (BFSK), Quadrature Phase Shift Keying (QPSK), Minimum Shift Keying (MSK)

[Handwritten signatures and marks at the bottom of the page]

Introduction to Error Control Coding: Linear Block Codes - Error detection & Error correction capabilities, Hamming Codes, Convolution Codes - Encoding, Tree and Trellis diagram, Decoding using Viterbi algorithm.

Text Books:

- [1] Simon Haykin and Michael Moher *Introduction to Analog and Digital Communications*, 2nd ed. United States of America: John Wiley & sons, inc., 2007. (Chapters: 3,4,5,6,7)
- [2] K. Sam Shanmugam, *Digital and Analog Communication Systems*, New Delhi: John Wiley & Sons, 2008. (Chapters: 4,5,8,9,10)

Reference Books:

- [1] Herbart Taub, Donald L Schilling, *Principles of Communication Systems*, McGraw-Hill, 3rd ed, 2007
- [2] John G. Proakis, *Digital Communications*, McGraw-Hill Education, 4th ed, 2001
- [3] Bhattacharya, *Digital Communication*, Tata McGraHill Education, 2014.

Course Learning Outcomes (COs):

On completion of this course, students will be able to...

CO1: estimate the performance of AM systems in the presence of noise

CO2: evaluate the performance of FM system in the presence of noise and discuss pulse modulation techniques

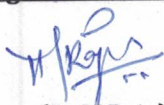
CO3: determine code efficiency of source coding algorithms and design the duo-binary filtering methods to reduce the effect of Inter Symbol Interference

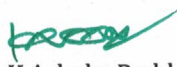
CO4: examine the performance of coherent bandpass data transmission system and design channel encoders & decoders

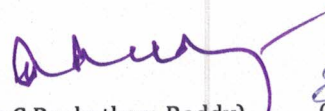
Course Articulation Matrix (CAM): U18EC503 COMMUNICATION SYSTEMS

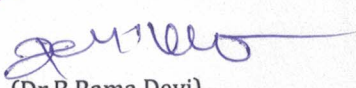
CO		PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PO 12	PSO 1	PSO 2
CO1	U18EC503.1	2	2	1	1	-	-	-	-	-	-	-	1	1	2
CO2	U18EC503.2	2	2	1	1	-	-	-	-	-	-	-	1	1	2
CO3	U18EC503.3	2	2	1	1	-	-	-	-	-	-	-	1	1	2
CO4	U18EC503.4	2	2	1	1	-	-	-	-	-	-	-	1	1	2
	U18EC503	2	2	1	1	-	-	-	-	-	-	-	1	1	2

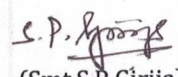
Signatures of Internal BoS Members:

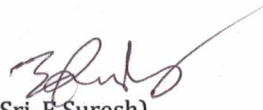

(Dr.M.Raju)
Chairperson, BoS, ECE



(Dr.K.Ashoka Reddy)
Member, BoS, ECE

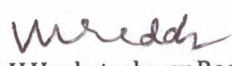

(Dr.G.Raghotham Reddy)
Member, BoS, ECE



(Dr.B.Rama Devi)
Member, BoS, ECE



(Smt.S.P.Girija)
Member, BoS, ECE


(Sri. E.Suresh)
Member, BoS, ECE



(Smt. A.Vijaya)
Co-Opted Member-1


(Dr.V.Venkateshwar Reddy)
Co-Opted Member-2


(Dr.K.Ramudu)
Special Invitee


(Sri. D.Venu)
Special Invitee


(Sri. R.Srikanth)
Special Invitee


(Sri. P.Chiranjeevi)
Special Invitee

U18EC605 VLSI CIRCUITS AND SYSTEMS

Class: B.Tech.VI – Semester

Branch: Electronics and Communication Engineering (ECE)

Teaching Scheme:

L	T	P	C
3	–	–	3

Examination Scheme:

Continuous Internal Evaluation	40 marks
End Semester Examination	60 marks

Course Learning Objectives(LOs):

This course will develop students' knowledge in/on...

LO1: *fabrication process and electrical properties of MOS transistors*

LO2: *stick diagrams, design rules, layout diagrams and basic circuit concepts of MOS transistors*

LO3: *data path subsystems using structured design principles*

LO4: *basic concepts of Verilog and description of various levels of abstraction*

UNIT-I (9)

Introduction to MOS Technology: Introduction to VLSI, Basic MOS transistor, Process steps in fabricating MOSFET, Fabrication process of nMOS, CMOS and BiCMOS transistors

Basic Electrical Properties of MOS Transistor: Drain to source current and voltage relation, Threshold voltage, Transconductance, Pass transistor, nMOS inverter, Pull up/Pull down ratios, Alternate forms of pull up, CMOS inverter, BiCMOS inverter, Latch-up in CMOS circuits

UNIT - II (9)

MOS Circuit Design Processes: MOS layers, Stick diagrams - nMOS design style and CMOS design style, Lambda based design rules and Layout diagrams

Basic Circuit Concepts: Sheet resistance, Area capacitances of layers, Delay unit, Inverter delays, Rise time and Fall time estimation

UNIT - III (9)

Data path Subsystems: Introduction, Addition/Subtraction, One/Zero Detectors, Comparators, Counters, Boolean logical operations, Coding, Shifters, Multiplication, Division and Parallel-prefix computations

Subsystem Design and Layout: Architectural Issues, Switch Logic, Gate Logic, Examples of Structured Design, Clocked Sequential Circuits and System Considerations

UNIT - IV (9)

Verilog HDL: Hierarchical Modeling Concepts, Basic concepts - Data types, Modules and ports, Gate level modeling, Dataflow modeling, Behavioral modeling, Design examples of Combinational and Sequential circuits, Switch level modeling, Tasks and Functions

Text Books:

- [1] Neil H. E. Weste, David Harris and Ayan Banerjee, *CMOS VLSI Design – A Circuits and Systems Perspective*, 3rd ed., New Delhi: Pearson Education, 2005. (Chapters 1 to 4, 8,9)
- [2] Douglas A Pucknell and Kamran Eshraghian, *Basic VLSI Design*, 3rd ed., New Delhi: PHI, 2008. (Chapters 1 to 6)
- [3] Samir Palnitkar, Peter Flake, *Verilog HDL –Guide to Digital Design and Synthesis*, Pearson Education, 3rd Edition, 2003. (PART-I: Chapters 2 to 8)

Reference Books:

- [1] John P Uyemura, *Chip Design for Submicron VLSI: CMOS Layout and Simulation*, 2nd ed., Thomson /Nelson, 2010

Course Learning Outcomes (COs):

On completion of this course, students will be able to...

CO1: discuss the concepts of oxidation, photolithography & deposition techniques used in the fabrication process and assess the basic electrical properties of MOS transistors

CO2: construct the stick diagrams & mask layouts using design rules and estimate the sheet resistance, area capacitances of layers & time delays of MOS transistors

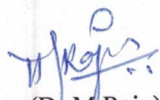
CO3: build the data path subsystems using structured design principles

CO4: develop Verilog programs for digital circuits using behavioral, dataflow, gate and switch levels of abstraction

Course Articulation Matrix (CAM):U18EC605 VLSI CIRCUITS AND SYSTEMS

CO	PO1	PO2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PO 12	PS O1	PS O2
CO1 U18EC605.1	2	2	1	1	--	1	1	1	1	1		1	2	2
CO2 U18EC605.2	2	2	1	1	--	1	1	1	1	1		1	2	2
CO3 U18EC605.3	2	2	1	1	--	1	1	1	1	1		1	2	2
CO4 U18EC605.4	2	1	1	1	1	1	1	1	1	1		1	2	2
U18EC605	2	1.75	1	1	1	1	1	1	1	1		1	2	2

Signatures of Internal BoS Members:



(Dr.M.Raju)
Chairperson, BoS, ECE



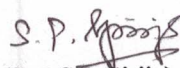
(Dr.K.Ashoka Reddy)
Member, BoS, ECE



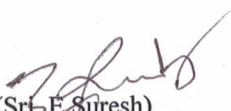
(Dr.G.Raghotham Reddy)
Member, BoS, ECE



(Dr.B.Rama Devi)
Member, BoS, ECE




(Smt.S.P.Girija)
Member, BoS, ECE



(Sri. E.Suresh)
Member, BoS, ECE



(Smt. A.Vijaya)
Co-Opted Member-1



(Dr.V.Venkateshwar Reddy)
Co-Opted Member-2



(Dr.K.Ramudu)
Special Invitee



(Sri. D.Venu)
Special Invitee



(Sri. R.Srikanth)
Special Invitee



(Sri. P.Chiranjeevi)
Special Invitee

U18EC606 EMBEDDED SYSTEMS WITH ARM PROCESSOR AND APPLICATIONS

Class: B.Tech.VI-Semester

Branch: Electronics and Communication Engineering (ECE)

Teaching Scheme:

L	T	P	C
3	-	-	3

Examination Scheme:

Continuous Internal Evaluation	40 marks
End Semester Examination	60 marks

Course Learning Objectives (LOs):

This course will develop students' knowledge in /on

LO1: structure of embedded systems and ARM controllers

LO2: instruction set and assembly language programming of ARM processor

LO3: ARM7 based microcontrollers, interfacing and programming

LO4: memory management in ARM

UNIT-I (9)

ARM Embedded Systems: Overview of Embedded System, Processor Embedded into a System, Classification of embedded systems. Embedded system hardware, embedded system software, the Acorn RISC Machine, RISC Design philosophy, ARM Design Philosophy, ARM processor families, Core extensions, Architecture revisions.

The ARM Architecture and Programmers Model: ARM Core data flow model, Architectural inheritance, The ARM7TDMI programmer's model: registers, CPSR, SPSR, The memory system, Pipeline, Exceptions, Interrupts and the vector table, load and store architecture, ARM development tools.

UNIT-II (9)

ARM Instruction set: Data processing instructions, Branch instructions, Load and store instructions, Software interrupt instructions, Program status register instructions, loading constants, Conditional execution Thumb instruction set: Thumb Register usage, Thumb Register Usage, ARM-Thumb Interworking and other Branch Instructions. Data Processing Instructions, Single-Register Load-Store Instructions, Multiple-Register Load-Store Instructions, Stack Instructions, Software Interrupt Instructions; advantage of thumb instructions, assembler rules and directives, Assembly language programs for shifting of data, factorial calculation, swapping register contents.

UNIT-III (9)

ARM7 Based Microcontroller LPC2148: Features, Applications, Block Diagram, memory mapping, Functional features of Interrupt controller, RTC, USB, UART, I2C, SPI, SSP controllers, watchdog timers and other system control units; Peripherals: Pin Connect Block- Features, Register description with example. GPIO-Features, Applications, Pin description, Register description with examples PLL-Features, block diagram, bit structure of PLLCON, PLLCFG, & PLLSTAT, and PLLFEED. PLL frequency Calculation- procedure for determining PLL settings, examples for PLL Configuration Timers-Features, applications, Architecture of timer module, register description.

Programming of LPC2148: C programs for General purpose I/O, interfacing with LED, LCD, KEYPAD, general purpose timer, PWM Modulator, UART, I2C Interface, SPI Interface, ADC, DAC.

UNIT-IV (9)

Memory management units: Moving from memory protection unit (MPU) to memory management unit (MMU), Working of virtual memory, Multitasking, Memory organization in virtual memory system, Page tables, Translation look aside buffer, Caches and write buffer, Fast context switch extension, Advanced Microprocessor Bus Architecture (AMBA) Bus System, User peripherals, Exception's handling in ARM.

CORTEX A8 ARM Processor based Beagle Bone: Beagle Bone Black Overview, Beagle Bone Black High Level Specification; Sitara AM3358BZCZ100 Processor.

[Handwritten signatures and marks at the bottom of the page]

Text Books:

- [1] Sloss, Andrew, Dominic Symes, and Chris Wright. ARM system developer's guide: designing and optimizing system software. Elsevier, 2004.
- [2] LPC2148 User manual
- [3] BeagleBone Black System Reference Manual

Reference Books:

- [1] Rajkamal, "Embedded Systems: Architecture, Programming and Design", TMH Publications, Second Edition, 2008.
- [2] Furber, Stephen Bo. ARM system-on-chip architecture, New Delhi: Pearson Education, 2000.
- [3] Mazidi, Muhammad Ali, et al. ARM Assembly Language Programming & Architecture (Volume 1). Micro Digital Ed. com, 2016.
- [4] Das, Lyla B. Embedded Systems: An Integrated Approach. Pearson Education India, 2012.

Course Learning Outcomes (COs):

After completion of this course, the students will be able to

CO1: examine the structure of embedded systems and ARM controllers

CO2: utilize the Instruction set for assembly language programming of ARM

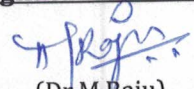
CO3: develop interfacing of various components/devices with ARM7 based microcontrollers

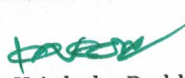
CO4: classify the memory management units in ARM

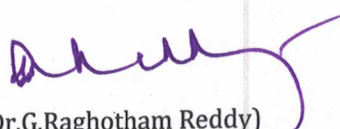
Course Articulation Matrix (CAM): U18EC606 EMBEDDED SYSTEMS WITH ARM PROCESSOR AND APPLICATIONS


CO		PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	U18EC606.1	2	2	1	2	2	-	-	-	-	-	1	2	1	2
CO2	U18EC606.2	2	2	2	2	2	-	-	-	-	-	1	1	1	2
CO3	U18EC606.3	2	2	2	2	2	-	-	-	-	-	1	2	1	2
CO4	U18EC606.4	2	2	2	2	2	-	-	-	-	-	1	1	2	2
U18EC606		2	2	1.75	2	2	-	-	-	-	-	1	1.5	1.25	2

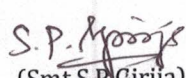
Signatures of Internal BoS Members:

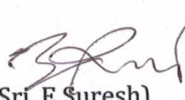

(Dr. M. Raju)
Chairperson, BoS, ECE



(Dr. K. Ashoka Reddy)
Member, BoS, ECE

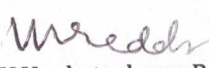

(Dr. G. Raghotham Reddy)
Member, BoS, ECE



(Dr. B. Rama Devi)
Member, BoS, ECE



(Smt. S. P. Girija)
Member, BoS, ECE



(Sri. E. Suresh)
Member, BoS, ECE



(Smt. A. Vijaya)
Co-Opted Member-1


(Dr. V. Venkateshwar Reddy)
Co-Opted Member-2


(Dr. K. Ramudu)
Special Invitee


(Sri. D. Venu)
Special Invitee


(Sri. R. Srikanth)
Special Invitee


(Sri. P. Chiranjeevi)
Special Invitee

P20SP201: SOFTWARE DEFINED RADIO

Class: M.Tech. II - Semester

Specialization: CESP

TeachingScheme:

L	T	P	C
3	-	-	3

ExaminationScheme:

Continuous Internal Evaluation	60 marks
End Semester Examination	40 marks

Course LearningObjectives(LOs):

This course will develop students' knowledge on /in...

LO1: design principles of software defined radio

LO2: business modelsfor Software-Defined Radio

LO3:radio frequency implementation issues in SDR

LO4: various techniques available to solve the problem of flexible and linear transmitter

UNIT-I (9)

Introduction to Software Radio Concepts: The need for software radios, definition of software radio, characteristics and benefits of a software radio, design principles of a software radio, software requirements and re-configurability, software defined radio architectures, required hardware specifications, digital aspects of a SDR, current technology limitations, impact of superconducting technologies on future SDR systems

UNIT-II (9)

Business Models for Software-Defined Radio- Introduction ,Base-Station Model , Impact of OBSAI and CPRI™ , Handset Model, New Base-Station and Network Architectures- Separation of Digital and RF , Tower-Top Mounting , BTS Hoteling, Smart Antenna Systems- Introduction , Smart Antenna System Architectures , Power Consumption Issues , Calibration Issues

UNIT-III (9)

Radio Frequency Implementation Issues: The purpose of the RF front-end, dynamic range: the principal challenge of receiver design, RF receiver front-end topologies, enhanced flexibility of the RF chain with software radios, importance of the components to overall performance, transmitter architectures and their issues, noise and distortion in the RF chain, ADC and DAC distortion

UNIT - IV (9)

Flexible Transmitters and PAs: Introduction, Differences in PA Requirements for Base Stations and Handsets- Comparison of Requirements , Linearisation and Operational Bandwidths, Linear Upconversion Architectures- Analogue Quadrature Upconversion, Quadrature Upconversion with Interpolation, Interpolated Bandpass Upconversion, Digital IF Upconversion, Multi-Carrier Upconversion, Weaver Up conversion, Constant-Envelope Upconversion Architectures- PLL-Based Reference or Divider Modulated Transmitter , PLL-Based Directly-Modulated VCO Transmitter

[Handwritten signatures and marks at the bottom of the page]

Text Books:

- [1] Jeffrey H. Reed, *Software Radio: A Modern Approach to Radio Engineering*, Pearson, 2002
 [2] P. Kenington, *RR- and Baseband Techniques for Software Defined Radio*, Artech House, 2005

Reference Books:

- [1] Tony J Roupheal, *RF and DSP for SDK*, Elsevier Newnes Press, 2008.


Course Learning Outcomes (COs):


On completion of this course, students will be able to...

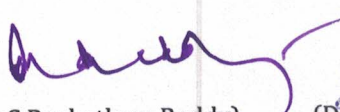
- [1] discuss software design aspects and reconfigurability of SDR
 [2] analyze the business models of software defined radio
 [3] elaborate radio frequency implementation issues in SDR
 [4] discuss various techniques available to solve the problem of flexible and linear transmitter

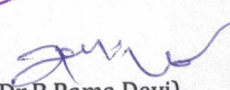
Course Articulation Matrix (CAM): P20SP201: SOFTWARE DEFINED RADIO						
CO		PO1	PO2	PO3	PSO1	PSO2
CO1	P20SP201.1	1	2	2	1	2
CO2	P20SP201.2	1	2	2	1	2
CO3	P20SP201.3	1	2	2	1	2
CO4	P20SP201.4	1	2	2	1	2
P20SP201		1	2	2	1	2

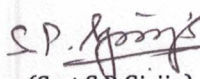
Signatures of Internal BoS Members:

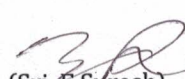

 (Dr. M. Raju)
 Chairperson, BoS, ECE

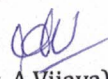

 (Dr. K. Ashoka Reddy)
 Member, BoS, ECE

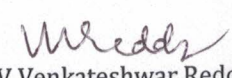

 (Dr. G. Raghotham Reddy)
 Member, BoS, ECE

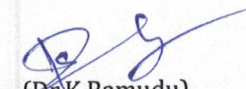

 (Dr. B. Rama Devi)
 Member, BoS, ECE



 (Smt. S. P. Girija)
 Member, BoS, ECE


 (Sri. E. Suresh)
 Member, BoS, ECE



 (Smt. A. Vijaya)
 Co-Opted Member-1


 (Dr. V. Venkateshwar Reddy)
 Co-Opted Member-2


 (Dr. K. Ramudu)
 Special Invitee


 (Sri. D. Venu)
 Special Invitee


 (Sri. R. Srikanth)
 Special Invitee


 (Sri. P. Chiranjeevi)
 Special Invitee



KAKATIYA INSTITUTE OF TECHNOLOGY & SCIENCE, WARANGAL-15

(An Autonomous Institute under Kakatiya University, Warangal)

No.KITS/Acad/Autonomous-BoS (ECE)/2020

Date: 07.03.2020

ORDERS

Sub: KITS, Warangal - UGC Autonomous status - Constitution of Board of Studies (BoS) for B. Tech. Electronics & Communication Engineering (ECE) Programme / M. Tech. Digital Communications (DC) Programme - Modified Orders - Issued.

- Ref: 1. Letter No. F. 22-1/2-14(AC), Dt. 19.6.2014 from the Joint Secretary, UGC, New Delhi.
2. Letter No. 350/CDC/KU/2014, Dt. 18.8.2014. from the Registrar, Kakatiya University, Warangal.
3. This office Order No. KITS/Acad/2014, Date: 20-8-2014.
4. Note No. 1113/ECE/KITS/2016, Date: 02-09-2016 from HOD, ECE
5. This office Order No.KITS/Acad/Autonomous-BoS(ECE)/2016, Date: 3.10.2016.
6. This office Order No.KITS/Acad/Autonomous-BoS(ECE)/2018, Date: 12.5.2018.
7. ECED office Note No. 77/ECE/KITS/2020, Date: 14.02.2020

In continuation of the order cited 6 above & with ref. to note 7 above, the Board of Studies (BoS) for B. Tech. Electronics & Communication Engineering (ECE) Programme / M. Tech. Digital Communications (DC) Programme has been constituted with the following members for a period of two (2) years with effect from the date of issue of these orders.

S. No.	Name of the Member	Designation	Position in BoS
1.	Dr. B. Rama Devi	Professor & HoD, ECED, KITSW	Chairperson, BoS
2.	Dr. K. Ashoka Reddy	Senior Professor of ECED, KITSW	Member
3.	Dr. G. Raghotham Reddy	Professor of ECED, KITSW	Member
4.	Smt. S. P. Girija	Assoc. Prof. of ECED, KITSW	Member
5.	Sri E. Suresh	Assoc. Prof. of ECED, KITSW	Member
6.	Sri Surya Kanth V Gangasetty	Professor, IIIT, Hyderabad	External Member (from renowned Academic Institute)
7.	Dr. L. Anjaneyulu	Professor & Head, Dept. of ECE, NIT, Warangal	External Member (from renowned Academic Institute)
8.	Dr. T. Srinivastulu	Professor, Dept. of ECE, KUCE, KU Dean, Faculty of Engineering, KU, Warangal	External Member (University Nominee)
9.	Sri Guntha Guptha	Senior Staff Engineer Manager, Qualcomm	External Member (from Industry)
10.	Dr. Vijender Basi Reddy	Scientist, ISRO, Hyderabad.	External Member (from Industry)
11.	Dr. G Sanath Kumar	Deputy Director, Central Institute of Tool Design (CITD), Hyderabad	External Member (from Industry)
12.	Sri V. Madhan Kumar	Lead Designer, Synopsys, Kondapur, Kothaguda, Hyderabad, Telangana (M.Tech 2009-11)	External Member (Post Graduate Meritorious Alumnus - Academia/Industry)
13.	Smt. A.Vijaya	Assoc. Prof. of ECED, KITSW	Co-Opted Member-1
14.	Dr. M. Raju	Assoc. Prof. of ECED, KITSW	Co-Opted Member-2
15.	Dr. V. Venkateshwar Reddy	Assoc. Prof. of ECED, KITSW	Co-Opted Member-3

The Board shall exercise such powers, perform such duties and functions in accordance with the procedure laid down in UGC norms for the Kakatiya Institute of Technology & Science, Warangal.

The meeting of the Board shall ordinarily be convened as and when necessary, at least twice in a year.

However, any member of the Board of Studies shall cease to be a member when he vacates the office, which he was holding at the time of his/her appointment, unless otherwise permitted by the authority.

To
The Persons concerned
Copy to: 1. Secretary & Correspondent 2. Treasurer 3. All Deans
4. All Heads of Departments 5. Academic Section

PRINCIPAL



KAKATIYA INSTITUTE OF TECHNOLOGY & SCIENCE, WARANGAL-15
(An Autonomous Institute under Kakatiya University, Warangal)

No.KITS/Acad/Autonomous-BoS (ECI)/2020

Date: 07.03.2020

ORDERS

- Sub: KITS, Warangal - UGC Autonomous status - Constitution of Board of Studies (BoS) for B. Tech. Electronics Communication & Instrumentation Engineering (ECI) Programme.
Ref: 1. Letter No. F. 22-1/2-14(AC), Dt. 19.6.2014 from the Joint Secretary, UGC, New Delhi.
2. Letter No. 350/CDC/KU/2014, Dt. 18.8.2014. from the Registrar, KU, Warangal.
3. ECED office Note No. 77/ECE/KITS/2020, Date: 14.02.2020

With ref. to note 3 cited above, the Board of Studies (BoS) for B. Tech. Electronics Communication & Instrumentation Engineering (ECI) Programme has been constituted with the following members for a period of two (2) years with effect from the date of issue of these orders.

S. No.	Name of the Member	Designation	Position in BoS
1.	Dr. B. Rama Devi	Professor & HoD, ECED, KITSW	Chairperson, BoS
2.	Dr. K. Ashoka Reddy	Senior Professor of ECED, KITSW	Member
3.	Dr. G. Raghotham Reddy	Professor of ECED, KITSW	Member
4.	Dr. K. Sivani	Professor of EIED, KITSW	Member
5.	Dr. K. Venumadhav	Professor of EIED, KITSW	Member
6.	Dr. P. Chandra Sekhar	Professor & Head, Dept. of ECE, University College of Engineering, O.U, Hyderabad	External Member (from renowned Academic Institute)
7.	Dr. T. Kishore Kumar	Professor, NIT, Warangal	External Member (from renowned Academic Institute)
8.	Dr. T. Srinivasulu	Professor, Dept. of ECE, KUCE, KU Dean, Faculty of Engineering, KU, Warangal	External Member (University Nominee)
9.	Dr. Y. Jagan Mohan Reddy	Senior Engineering Manager, Honewell Technology Solutions Labs Pvt Ltd, Hyderabad	External Member (from Industry)
10.	Sri R. Dileep	Sr. ASIC Design Engineer, Synopsis Inc, Pvt Ltd, Hyderabad	External Member (from Industry)
11.	Sri Bhaskar	Senior Staff Engineer Manager, Qualcomm	External Member (from Industry)
12.	Sri Gopi	Intel, Hyderabad	External Member (Post Graduate Meritorious Alumnus - Academia/Industry)
13.	Smt. M. Sreelatha	Professor of EIED, KITSW	Co-Opted Member-1
14.	Smt. S.P. Girija	Assoc. Prof. of ECED, KITSW	Co-Opted Member-2
	Sri E. Suresh	Assoc. Prof. of ECED, KITSW	Co-Opted Member-3

The Board shall exercise such powers, perform such duties and functions in accordance with the procedure laid down in UGC norms for the Kakatiya Institute of Technology & Science, Warangal.

The meeting of the Board shall ordinarily be convened as and when necessary, at least twice in a year.

However, any member of the Board of Studies shall cease to be a member when he vacates the office, which he was holding at the time of his/her appointment, unless otherwise permitted by the authority.

To
The Persons concerned
Copy to: 1. Secretary & Correspondent 2. Treasurer 3. All Deans
4. All Heads of Departments 5. Academic Section

PRINCIPAL

KAKATIYA INSTITUTE OF TECHNOLOGY & SCIENCE, WARANGAL-15
(An Autonomous Institute under Kakatiya University, Warangal)
DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

No. 77/ECE/KITS/2020

Date: 14.02.2020

Submitted to the Principal:

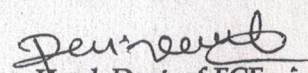
Sub: Nomination of **Internal members, External members (from Industry) and External member (Post Graduate Meritorious Alumnus – Industry/Academia) - Constitution of Board of Studies (BoS) for B.Tech. Electronics & Communication Engineering (ECE) Programme – Reg.**

Ref : 1. Office Order No. KITS/ Acad/ Autonomous-BoS (ECE)/2018, Date: 12.5.2018

Ref: 2. No. KITS/ Acad/ Autonomous-BoS (ECE)/2020, dated on 31.01.2020

With reference to the above cited letter the following members nominated for the department Board of Studies (BoS) of B.Tech. ECE Department, KITS, Warangal.

S. No.	Name of the Member	Designation	Position in BoS
1.	Dr. B. Rama Devi	HoD ECE, KITSW	Chairperson, BoS
2.	Dr. K. Ashoka Reddy	Senior Professor of ECE Dept. KITSW	Member
3.	Dr. G. Raghotham Reddy	Professor of ECE Dept. KITSW	Member
4.	S. P. Girija	Assoc. Prof. of ECE Dept. KITSW	Member
5.	E. Suresh	Assoc. Prof. of ECE Dept. KITSW	Member
6.	Surya Kanth V Gangasetty	Professor, IIIT, Hyderabad,	External Member (from renowned Academic Institute)
7.	Dr.L.Anjaneyulu	Professor & Head, Dept. of ECE, NIT, Warangal	External Member (from renowned Academic Institute)
8.	Prof. T. Srinivasulu	Professor, Dept. of ECE, KUCE, KU Dean, Faculty of Engineering, KU, Warangal	External Member (University Nominee)
9.	S.Venkateshwar Rao	AMD India Pvt.Ltd. Hyderabad, HITEC City, Madhapur, Hyderabad, Telangana	External Member (from Industry)
10.	Dr. Vijender Basi Reddy	Scientist, ISRO, Hyderabad.	External Member (from Industry)
11.	Dr. G Sanath Kumar,	Deputy Director, Central Institute of Tool Design (CITD), Hyderabad	External Member (from Industry)
12.	V.Madhan Kumar	Lead Designer, Synopsys, Kondapur, Kothaguda, Hyderabad, Telangana (M.Tech 2009-11)	External Member (Post Graduate Meritorious Alumnus – Academia/Industry)
13.	A.Vijaya	Assoç. Prof. of ECE Dept. KITSW	Co-Opted Member-1
14.	Dr. M. Raju	Assoc. Prof. of ECE Dept. KITSW	Co-Opted Member-2
15.	Dr. V.Venkateshwar Reddy	Assoc. Prof. of ECE Dept. KITSW	Co-Opted Member-3


Head, Dept. of ECE

KAKATIYA INSTITUTE OF TECHNOLOGY & SCIENCE, WARANGAL-15
(An Autonomous Institute under Kakatiya University, Warangal)

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

No. 77/ECE/KITS/2020

Date: 14.02.2020

Submitted to the Principal:

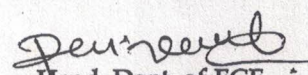
Sub: Nomination of Internal members, External members (from Industry) and External member (Post Graduate Meritorious Alumnus – Industry/Academia) - Constitution of Board of Studies (BoS) for B.Tech. Electronics & Communication Engineering (ECE) Programme – Reg.

Ref : 1. Office Order No. KITS/Acad/Autonomous-BoS (ECE)/2018, Date: 12.5.2018

Ref: 2. No. KITS/Acad/Autonomous-BoS (ECE)/2020, dated on 31.01.2020

With reference to the above cited letter the following members nominated for the department Board of Studies (BoS) of B.Tech. ECE Department, KITS, Warangal.

S. No.	Name of the Member	Designation	Position in BoS
1.	Dr. B. Rama Devi	HoD ECE, KITSW	Chairperson, BoS
2.	Dr. K. Ashoka Reddy	Senior Professor of ECE Dept. KITSW	Member
3.	Dr. G. Raghotham Reddy	Professor of ECE Dept. KITSW	Member
4.	S. P. Girija	Assoc. Prof. of ECE Dept. KITSW	Member
5.	E. Suresh	Assoc. Prof. of ECE Dept. KITSW	Member
6.	Surya Kanth V Gangasetty	Professor, IIIT, Hyderabad,	External Member (from renowned Academic Institute)
7.	Dr.L.Anjaneyulu	Professor & Head, Dept. of ECE, NIT, Warangal	External Member (from renowned Academic Institute)
8.	Prof. T. Srinivasulu	Professor, Dept. of ECE, KUCE, KU Dean, Faculty of Engineering, KU, Warangal	External Member (University Nominee)
9.	S.Venkateshwar Rao	AMD India Pvt.Ltd. Hyderabad, HITEC City, Madhapur, Hyderabad, Telangana	External Member (from Industry)
10.	Dr. Vijender Basi Reddy	Scientist, ISRO, Hyderabad.	External Member (from Industry)
11.	Dr. G Sanath Kumar,	Deputy Director, Central Institute of Tool Design (CITD), Hyderabad	External Member (from Industry)
12.	V.Madhan Kumar	Lead Designer, Synopsys, Kondapur, Kothaguda, Hyderabad, Telangana (M.Tech 2009-11)	External Member (Post Graduate Meritorious Alumnus – Academia/Industry)
13.	A.Vijaya	Assoc. Prof. of ECE Dept. KITSW	Co-Opted Member-1
14.	Dr. M. Raju	Assoc. Prof. of ECE Dept. KITSW	Co-Opted Member-2
15.	Dr. V.Venkateshwar Reddy	Assoc. Prof. of ECE Dept. KITSW	Co-Opted Member-3


Head, Dept. of ECE

Prof. K. Purushotham
MA.PGDTE, M.Phil, Ph.D
REGISTRAR &
Professor of English



KAKATIYA UNIVERSITY
Acredited with 'A' Grade by NAAC
Vidyanarayapuri, WARANGAL – 506 009
Telangana – INDIA

No. 726/B2/KU/2018

May 7, 2018

To
The Principal
Kakatiya Institute of Technology & Science (Autonomous)
Yerragattugutta, Hanamkonda 506 015

Sub: Kakatiya Institute of Technology and Science (KITS), WARANGAL
– Board of Studies (BoS) – Nomination of Members for various
Departments – Regarding

Ref: Your Letter No. KITS/Acad/UGC-A/2015, dated: 13.10.2017

Sir,

Apropos of your letter cited, I am to inform you that the Vice-Chancellor has nominated the following subject experts as University nominee to the Boards of Studies in various Departments/Courses at your college:

#	Department / Course	Nominated Teacher
1.	Civil Engineering	Dr. B. Sesha Srinivasa Rao Professor, University College of Engineering, Kothagudem
2.	Mechanical Engineering	Prof. Sriram Venkatesh Professor, MED, Department of Mechanical Engineering, Osmania University, Hyderabad
3.	Electronics & Instrumentation Engineering	Dr. K. Bhikshalu Assistant Professor of ECE, University College of Engineering, Kothagudem
4.	Electrical & Electronics Engineering	Dr. M. Shailaka Kumari Associate Professor, Department of Electrical Engineering, National Institute of Technology (NIT), Warangal
5.	Computer Science and Engineering	Dr. M. Sadanandam Department of Computer Science & Engineering, KU College of Engineering & Technology, Kakatiya University, Warangal
6.	Electronics and Communication Engineering	Prof. T. Srinivasulu Prof. & Dean, KU College of Engineering & Technology, Kakatiya University, Warangal

U18EC502A ARTIFICIAL INTELLIGENCE AND MACHINE LEARNING WITH PYTHON

Class: B.Tech. V – Semester**Branch:** Electronics and Communication Engineering (ECE)**Teaching Scheme:****Examination Scheme:**

L	T	P	C
3	-	-	3

Continuous Internal Evaluation	40 marks
End Semester Examination	60 marks

Course Learning Objectives (LOs):

This course will develop students' knowledge on /in...

LO1: artificial intelligence and machine learning

LO2: python fundamentals

LO3: python programming for machine learning algorithms

LO4: deep learning and optimization algorithms

UNIT-I (9)

AIML fundamentals: Artificial intelligence-definition, applications, advantages and disadvantages; machine learning - definition, application and types of learning - supervised learning, unsupervised learning, reinforcement learning, supervised and unsupervised machine learning algorithms; artificial neural network - perceptron, feed forward back propagation architecture, deep neural network and Python IDEs

UNIT-II (9)

Python fundamentals: Variables, data types - numeric, string, list, dictionary, tuple and set; arrays, indentation, operators, conditional statements, loops, functions, numpy, arrays and data frames using pandas, data visualization using matplotlib - plot, histogram, bar graphs and scatter diagram; data visualization using sea borne library and waveform generation-sine, cosine and sinc functions

UNIT-III (9)

Machine learning algorithms and Python programming: Scikit learn, regression-simple linear regression, multiple linear regression, polynomial regression and importance of R^2 value in regression; clustering -hierarchical, k-means, density based and fuzzy clustering; classification - logistic regression, support vector machine, naïve bayes algorithm, decision tree and random forest algorithm

UNIT-IV (9)

Deep learning: Convolutional neural network, recurrent neural network, natural language processing (NLP) - components, applications and NLTK library; open cv library for image processing and chat bots

Optimization algorithms: Genetic algorithm and particle swarm optimization algorithm

U18EC502A ARTIFICIAL INTELLIGENCE AND MACHINE LEARNING WITH PYTHON

Class: B.Tech. V – Semester

Branch: Electronics and Communication Engineering (ECE)

Teaching Scheme:

Examination Scheme:

L	T	P	C
3	-	-	3

Continuous Internal Evaluation	40 marks
End Semester Examination	60 marks

Course Learning Objectives (LOs):

This course will develop students' knowledge on /in...

LO1: machine learning-supervised, unsupervised and reinforcement learning and deep learning and its applications

LO2: python fundamentals on variables, data types, data structures, loops and file handling, arrays and data frames using NumPy and pandas

LO3: machine learning models, regression techniques, clustering techniques and classification techniques

LO4: artificial, convolutional and recurrent deep learning and neural networks, object detection, facial recognition, video analytics using open CV library for image processing and natural language processing

UNIT-I (9)

Introduction To Machine Learning & Artificial Intelligence: What is Machine Learning (ML); Types – supervised, semi supervised, unsupervised and reinforcement learning; Use cases in different verticals – Banking, Entertainment, Marketing and Smart devices; What is Artificial Intelligence (AI); Ethics in AI; Deep learning and applications

UNIT - II (9)

Introduction to Python for ML & AI: Python and why it is preferred in AI and ML; Python Interpreter and IDE; Python fundamentals – Variables, Data types, Data structures, OOPs, loops and File handling; Arrays and data frames using NumPy and Pandas; Data mining methodology – CRISPDM, data wrangling, descriptive statistics and Data visualization – Matplotlib and seaborn packages

UNIT - III (9)

Python for Machine Learning – Scientific Libraries: ML models - Introduction to Scikit learn; Regression techniques – simple and multi linear regression, Polynomial regression, logistic regression; Clustering techniques – hierarchical and density based; Classification techniques – decision trees and random forest, Naïve Bayes, Model Evaluation techniques and accuracy in different models, ML with predictive maintenance from MATLAB toolbox

UNIT - IV (9)

Python for Artificial Intelligence: Deep Learning and Neural networks – artificial, convolutional and recurrent; Computer vision – open CV library for image processing, object detection, facial recognition, video analytics; Natural language Processing – NLTK library; Speech to text, text to speech, sequence to sequence modeling and Chatbots

U18EC702A DATA SCIENCE AND ENGINEERING*(Professional Elective – III)***Class:** B.Tech.VII – Semester**Branch:** Electronics and Communication Engineering**Teaching Scheme:**

L	T	P	C
3	-	-	3

Examination Scheme:

Continuous Internal Evaluation	40 marks
End Semester Examination	60 marks

Course Learning Objectives:

This course will develop students' knowledge in/on

- LO1: Relating the probabilistic views for analyzing data by using statistical principles.
 LO2: Understanding the basic terminology and syntaxes using Python-NumPy
 LO3: Applications of statistical principles for data handling, manipulation and visualization.
 LO4: Development of Machine learning algorithms for various applications

UNIT – I(9)

Introduction to Data Science- Basic Probability Theory, Random Variables, Expectation, Random Processes, Descriptive statistics, Need for Data Science, Life Cycle Phases of Data Analytics.

UNIT – II (9)

Introduction to NumPy-Understanding Data Types in Python, NumPy Arrays, Computation on NumPy Arrays, Aggregations, Computation on Arrays, Comparisons, Masks, and Boolean Logic, Fancy Indexing, Sorting Arrays, Structured Data

UNIT – III (9)

Data Manipulation with Pandas- Introducing Pandas Objects, Data Indexing and Selection, Operating on Data in Pandas, Handling Missing Data, Hierarchical Indexing, Combining Datasets, Aggregation and Grouping, Pivot Tables, Vectorized String Operations, Working with Time Series, High-Performance Pandas

Visualization with Matplotlib- General Matplotlib, Two Interfaces for the Price of One, Simple Line Plots, Visualizing Errors, Density and Contour Plots, Histograms, Binnings, and Density, Customizing Matplotlib, Three-Dimensional Plotting in Matplotlib, Geographic Data with Basemap, Visualization with Seaborn.

UNIT – IV (9)

Machine Learning- Introduction, Introducing Scikit-Learn, Hyper parameters and Model Validation, Feature Engineering, Naive Bayes Classification, Linear Regression, Support Vector Machine, Decision Tree and Random forest, Principal Component Analysis, Manifold Learning, k-Means Clustering

Case study: Powerful Data Collection Tools in Healthcare open link, A Face Detection Pipeline.

Textbook:

- [1]. Carlos Fernandez-Granda, *Probability and Statistics for Data Science*, NYU, New York, August 2017.
- [2]. Jake VanderPlas, *Phyton Data Science Handook-Essential Tools For Working With Data* O'Reilly Media, First Edition, 2017.
- [3]. Michael Mitzenmacher and Eli Upfal; *Probability and Computing*, 2ed ,Cambridge University

U18EC702A DATA SCIENCE ENGINEERING

(Professional Elective-III)

Class: B.Tech.VII – Semester

Branch: Electronics & Communications Engineering (ECE)

Teaching Scheme:

Examination Scheme:

L	T	P	C
3	-	-	3

Continuous Internal Evaluation	40 marks
End Semester Examination	60 marks

Course Learning Objectives:

This course will develop students' knowledge in/on

LO1: R as a programming language

LO2: data handling procedures using R

LO3: quadratic problem solving and Bayes theorem

LO4: the Bass model, discriminant & factor analysis and classical natural language processing

UNIT - I(9)

Data Science Modeling in R : System commands, loading data, matrices, descriptive statistics, higher-order moments, quick introduction to brownian motions with R, estimation using maximum-likelihood, garch/arch models, introduction to montecarlo, portfolio computations in R, finding the optimal portfolio, root solving, regression, heteroskedasticity, auto-regressive models, vector auto-regression

UNIT - II (9)

Data Handling Procedure: Data extraction of stocks using quantmod, using the merge function, using the apply class of functions, getting interest rate data from fred, cross-sectional data (an example), handling dates with lubridate, using the data table package, another data set: bay area bike share data, using the plyr package family

UNIT - III (9)

Markowitz Optimization: Quadratic (Markowitz) problem, solution in R, solving the problem with the quadprog package, tracing out the efficient frontier, covariances of frontier portfolios: rp,rq, combinations, zero covariance portfolio, portfolio problems with riskless assets, risk budgeting

Bayes Theorem: Introduction, Bayes and joint probability distributions, correlated default (conditional default), continuous and more formal exposition, Bayes nets, bayes rule in marketing

UNIT - IV (9)

The Bass Model: Introduction, historical examples, the basic idea, solving the model, symbolic math in R

Discriminant and Factor Analysis: Overview, discriminant analysis, discriminant function, caveats, implementation using R, confusion matrix, multiple groups, eigen systems, factor analysis, principal components analysis (PCA), classical approaches to natural language processing, text preprocessing, lexical analysis, syntactic parsing

Textbook:

- [1] Avrim Blum, John Hopcroft, and RavindranKannan, *Foundations of Data Science*, USA: Cambridge University Press, 2018.
- [2] SanjeevRanjan Das, *Data Science: Theories, Models, Algorithms, and Analytics*, New Delhi: S.R. Das, 2017.

KAKATIYA INSTITUTE OF TECHNOLOGY & SCIENCE: WARANGAL-15
DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

Date: 20.01.2022

Submitted to the Principal


Sub: Modification of Syllabus - U18EC606 EMBEDDED SYSTEMS WITH ARM PROCESSOR AND APPLICATIONS


Pl. find as attachment the modified syllabus of U18EC606 EMBEDDED SYSTEMS WITH ARM PROCESSOR AND APPLICATIONS, We are attaching the OLD and NEW syllabus for your reference.

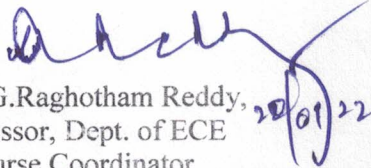
It is to bring to your notice that unnecessary content in the sequence of flow is removed and necessary content to be taught is added during modification, In total 10% of the syllabus content is moderated for proper understanding of the students without changing the total teaching contact hours.

The syllabi will be available in one text book and company user manuals.

This is for your favour of information and necessary initiation.


Sri. D. Santhosh Kumar
Asst. Prof, Dept. of ECE
CC Member


Smt. S.P. Girija
Assoc. Prof, Dept. of ECE
CC Member


Dr. G. Raghotham Reddy,
Professor, Dept. of ECE
Course Coordinator

U18EC606 EMBEDDED SYSTEMS WITH ARM PROCESSOR AND APPLICATIONS

Class: B.Tech.VI-Semester

Branch: Electronics and Communication Engineering (ECE)

Teaching Scheme:

L	T	P	C
3	-	-	3

Examination Scheme:

Continuous Internal Evaluation	40 marks
End Semester Examination	60 marks

Course Learning Objectives (LOs):

This course will develop students' knowledge in /on

LO1: structure of embedded systems and ARM controllers

LO2: instruction set and assembly language programming of ARM processor

LO3: ARM7 based microcontrollers, interfacing and programming

LO4: memory management in ARM

UNIT-I (9)

ARM Embedded Systems: Overview of Embedded System, Processor Embedded into a System, Classification of embedded systems. Embedded system hardware, embedded system software, the Acorn RISC Machine, RISC Design philosophy, ARM Design Philosophy, ARM processor families, Core extensions, Architecture revisions.

The ARM Architecture and Programmers Model: ARM Core data flow model, Architectural inheritance, The ARM7TDMI programmer's model: registers, CPSR, SPSR, The memory system, Pipeline, Exceptions, Interrupts and the vector table, load and store architecture, ARM development tools.

UNIT-II (9)

ARM Instruction set: Data processing instructions, Branch instructions, Load and store instructions, Software interrupt instructions, Program status register instructions, loading constants, Conditional execution Thumb instruction set: Thumb Register usage, Thumb Register Usage, ARM-Thumb Interworking and other Branch Instructions. Data Processing Instructions, Single-Register Load-Store Instructions, Multiple-Register Load-Store Instructions, Stack Instructions, Software Interrupt Instructions; advantage of thumb instructions, assembler rules and directives, Assembly language programs for shifting of data, factorial calculation, swapping register contents.

UNIT-III (9)

ARM7 Based Microcontroller LPC2148: Features, Applications, Block Diagram, memory mapping, Functional features of Interrupt controller, RTC, USB, UART, I2C, SPI, SSP controllers, watchdog timers and other system control units; Peripherals: Pin Connect Block- Features, Register description with example. GPIO-Features, Applications, Pin description, Register description with examples PLL-Features, block diagram, bit structure of PLLCON, PLLCFG, & PLLSTAT, and PLLFEED. PLL frequency Calculation- procedure for determining PLL settings, examples for PLL Configuration Timers-Features, applications, Architecture of timer module, register description.

Programming of LPC2148: C programs for General purpose I/O, interfacing with LED, LCD, KEYPAD, general purpose timer, PWM Modulator, UART, I2C Interface, SPI Interface, ADC, DAC.

UNIT-IV (9)

Memory management units: Moving from memory protection unit (MPU) to memory management unit (MMU), Working of virtual memory, Multitasking, Memory organization in virtual memory system, Page tables, Translation look aside buffer, Caches and write buffer, Fast context switch extension, Advanced Microprocessor Bus Architecture (AMBA) Bus System, User peripherals, Exception's handling in ARM.

CORTEX A8 ARM Processor based Beagle Bone: Beagle Bone Black Overview, Beagle Bone Black High Level Specification; Sitara AM3358BZCZ100 Processor.

U18EC606 EMBEDDED SYSTEMS WITH ARM PROCESSOR AND APPLICATIONS

Class: B.Tech. VI-Semester

Branch: Electronics and Communication Engineering (ECE)

Teaching Scheme :

L	T	P	C
3	-	-	3

Examination Scheme :

Continuous Internal Evaluation	40 marks
End Semester Examination	60 marks

Course Learning Objectives (LOs):

This course will develop students' knowledge in /on

LO1: structure of embedded systems and ARM controllers

LO2: instruction set and assembly language programming of ARM processor

LO3: ARM7 based microcontrollers, interfacing and programming

LO4: memory management in ARM

UNIT-I (9)

Introduction to Embedded Systems: Overview of Embedded Systems, Processor Embedded into a system, Embedded Hardware Units and Devices in system, Embedded Software, Complex System Design, Design Process in Embedded System, Formalization of System Design, and Classification of Embedded Systems; Embedded Processors: PSOC (Programmable System-on Chip) architectures, Continuous Timer blocks, Switched Capacitor blocks, I/O blocks, Digital blocks, Programming of PSOC

Introduction to ARM: Need of advanced microprocessors, Difference between RISC and CISC, RISC Design philosophy, ARM Design Philosophy, History of ARM microprocessor, ARM processor family, Development of ARM architecture. The ARM Architecture and Programmers Model : The Acorn RISC Machine, ARM Core data flow model, Architectural inheritance, The ARM7TDMI programmer's model: General purpose registers, CPSR, SPSR, ARM memory map, data format, load and store architecture, Core extensions, Architecture revisions, Exception Levels, ARM development tools

UNIT-II (9)

ARM Instruction set: Data processing instructions, Arithmetic and logical instructions, Rotate and barrel shifter, Branch instructions, Load and store instructions, Software interrupt instructions, Program status register instructions, Conditional execution, Multiple register load and store instructions, Stack instructions, Thumb instruction set, advantage of thumb instructions, Assembler rules and directives, Assembly language programs for shifting of data, factorial calculation, swapping register contents, moving values between integer and floating point registers, Virtualization

UNIT-III (9)

ARM7 Based Microcontroller LPC2148: Features, Architecture (Block Diagram and Its Description), System Control Block (PLL and VPB divider) , Memory Map, GPIO, Pin Connect Block, timer, interfacing with LED, LCD, KEYPAD

C Programming for ARM: Overview of C compiler and optimization, Basic C data types, C Looping structures, Register allocations, function calls, pointer aliasing, structure arrangement, bitfields, unaligned data and Endianness, Division, floating point, Inline functions and inline assembly, Portability issues. C programs for 10 20 General purpose I/O, general purpose timer, PWM Modulator, UART, I2C Interface, SPI Interface, ADC, DAC

KAKATIYA INSTITUTE OF TECHNOLOGY & SCIENCE: WARANGAL-15
DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

Date: 22.01.2022

Submitted to the Principal

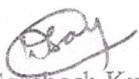
Sub: Modification of Syllabus - U18EC606 EMBEDDED SYSTEMS WITH ARM PROCESSOR AND APPLICATIONS

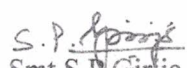
Pl. find as attachment the modified syllabus of U18EC606 EMBEDDED SYSTEMS WITH ARM PROCESSOR AND APPLICATIONS, We are attaching the OLD and NEW syllabus for your reference.

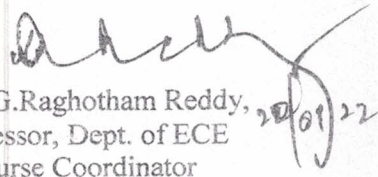
It is to bring to your notice that unnecessary content in the sequence of flow is removed and necessary content to be taught is added during modification, In total 10% of the syllabus content is moderated for proper understanding of the students without changing the total teaching contact hours.

The syllabi will be available in one text book and company user manuals.

This is for your favour of information and necessary initiation.


Sri. D. Santhosh Kumar
Asst. Prof, Dept. of ECE
CC Member


Smt. S.R. Girija
Assoc. Prof, Dept. of ECE
CC Member


Dr. G. Raghotham Reddy,
Professor, Dept. of ECE
Course Coordinator

U18EC606 EMBEDDED SYSTEMS WITH ARM PROCESSOR AND APPLICATIONS

Class: B.Tech.VI-Semester

Branch: Electronics and Communication Engineering (ECE)

Teaching Scheme:

L	T	P	C
3	-	-	3

Examination Scheme:

Continuous Internal Evaluation	40 marks
End Semester Examination	60 marks

Course Learning Objectives (LOs):

This course will develop students' knowledge in /on

LO1: structure of embedded systems and ARM controllers

LO2: instruction set and assembly language programming of ARM processor

LO3: ARM7 based microcontrollers, interfacing and programming

LO4: memory management in ARM

UNIT-I (9)

ARM Embedded Systems: Overview of Embedded System, Processor Embedded into a System, Classification of embedded systems. Embedded system hardware, embedded system software, the Acorn RISC Machine, RISC Design philosophy, ARM Design Philosophy, ARM processor families, Core extensions, Architecture revisions.

The ARM Architecture and Programmers Model: ARM Core data flow model, Architectural inheritance, The ARM7TDMI programmer's model: registers, CPSR, SPSR, The memory system, Pipeline, Exceptions, Interrupts and the vector table, load and store architecture, ARM development tools.

UNIT-II (9)

ARM Instruction set: Data processing instructions, Branch instructions, Load and store instructions, Software interrupt instructions, Program status register instructions, loading constants, Conditional execution Thumb instruction set: Thumb Register usage, Thumb Register Usage, ARM-Thumb Interworking and other Branch Instructions. Data Processing Instructions, Single-Register Load-Store Instructions, Multiple-Register Load-Store Instructions, Stack Instructions, Software Interrupt Instructions; advantage of thumb instructions, assembler rules and directives, Assembly language programs for shifting of data, factorial calculation, swapping register contents.

UNIT-III (9)

ARM7 Based Microcontroller LPC2148: Features, Applications, Block Diagram, memory mapping, Functional features of Interrupt controller, RTC, USB, UART, I2C, SPI, SSP controllers, watchdog timers and other system control units; Peripherals: Pin Connect Block- Features, Register description with example. GPIO-Features, Applications, Pin description, Register description with examples PLL-Features, block diagram, bit structure of PLLCON, PLLCFG, & PLLSTAT, and PLLFEED. PLL frequency Calculation- procedure for determining PLL settings, examples for PLL Configuration Timers-Features, applications, Architecture of timer module, register description.

Programming of LPC2148: C programs for General purpose I/O, interfacing with LED, LCD, KEYPAD, general purpose timer, PWM Modulator, UART, I2C Interface, SPI Interface, ADC, DAC.

UNIT-IV (9)

Memory management units: Moving from memory protection unit (MPU) to memory management unit (MMU), Working of virtual memory, Multitasking, Memory organization in virtual memory system, Page tables, Translation look aside buffer, Caches and write buffer, Fast context switch extension, Advanced Microprocessor Bus Architecture (AMBA) Bus System, User peripherals, Exception's handling in ARM.

CORTEX A8 ARM Processor based Beagle Bone: Beagle Bone Black Overview, Beagle Bone Black High Level Specification; Sitara AM3358BZCZ100 Processor.

U18EC606 EMBEDDED SYSTEMS WITH ARM PROCESSOR AND APPLICATIONS

Class: B.Tech. VI-Semester

Branch: Electronics and Communication Engineering (ECE)

Teaching Scheme :

L	T	P	C
3	-	-	3

Examination Scheme :

Continuous Internal Evaluation	40 marks
End Semester Examination	60 marks

Course Learning Objectives (LOs):

This course will develop students' knowledge in / on

LO1: structure of embedded systems and ARM controllers

LO2: instruction set and assembly language programming of ARM processor

LO3: ARM7 based microcontrollers, interfacing and programming

LO4: memory management in ARM

UNIT-I (9)

Introduction to Embedded Systems: Overview of Embedded Systems, Processor Embedded into a system, Embedded Hardware Units and Devices in system, Embedded Software, Complex System Design, Design Process in Embedded System, Formalization of System Design, and Classification of Embedded Systems; Embedded Processors: PSOC (Programmable System-on Chip) architectures, Continuous Timer blocks, Switched Capacitor blocks, I/O blocks, Digital blocks, Programming of PSOC

Introduction to ARM: Need of advanced microprocessors, Difference between RISC and CISC, RISC Design philosophy, ARM Design Philosophy, History of ARM microprocessor, ARM processor family, Development of ARM architecture. The ARM Architecture and Programmers Model : The Acorn RISC Machine, ARM Core data flow model, Architectural inheritance, The ARM7TDMI programmer's model: General purpose registers, CPSR, SPSR, ARM memory map, data format, load and store architecture, Core extensions, Architecture revisions, Exception Levels, ARM development tools

UNIT-II (9)

ARM Instruction set: Data processing instructions, Arithmetic and logical instructions, Rotate and barrel shifter, Branch instructions, Load and store instructions, Software interrupt instructions, Program status register instructions, Conditional execution, Multiple register load and store instructions, Stack instructions, Thumb instruction set, advantage of thumb instructions, Assembler rules and directives, Assembly language programs for shifting of data, factorial calculation, swapping register contents, moving values between integer and floating point registers, Virtualization

UNIT-III (9)

ARM7 Based Microcontroller LPC2148: Features, Architecture (Block Diagram and Its Description), System Control Block (PLL and VPB divider) , Memory Map, GPIO, Pin Connect Block, timer, interfacing with LED, LCD, KEYPAD

C Programming for ARM: Overview of C compiler and optimization, Basic C data types, C Looping structures, Register allocations, function calls, pointer aliasing, structure arrangement, bitfields, unaligned data and Endianness, Division, floating point, Inline functions and inline assembly, Portability issues. C programs for 10 20 General purpose I/O, general purpose timer, PWM Modulator, UART, I2C Interface, SPI Interface, ADC, DAC

KAKATIYA INSTITUTE OF TECHNOLOGY & SCIENCE, WARANGAL
DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

Date:07.02.2022

Submitted to the Principal

Sub: Modification of Syllabus-U18EC503 COMMUNICATION SYSTEMS


PI find as attachment the modified syllabus of U18EC503 COMMUNICATION SYSTEMS, we are attaching the OLD and NEW syllabus for your reference.

It is to bring to your notice that unnecessary content in the sequence of flow is removed and necessary content is added during modification. In total 10% of the syllabus content is moderated for proper understanding of the students without changing the total teaching contact hours.

This is for your favour of information and necessary initiation.



Dr K. Sowjanya
Asst. Prof, Dept. of ECE
CC Member



Dr K. Ramudu
Asst. Prof, Dept. of ECE
CC Member



Dr M. Raju
Assoc. Prof, Dept. of ECE
CC Member

U18EC503 COMMUNICATION SYSTEMS

Class: B.Tech. V - Semester

Branch: Electronics and Communication Engineering (ECE)

Teaching Scheme:

L	T	P	C
3	-	-	3

Examination Scheme:

Continuous Internal Evaluation	40 marks
End Semester Examination	60 marks

Course Learning Objectives (LOs):

This course will develop students' knowledge on /in...

LO1: linear modulation strategies that constitute the amplitude modulation

LO2: angle modulation & pulse modulation

LO3: source coding, digital modulation techniques & baseband data transmission systems

LO4: bandpass data transmission systems & channel coding techniques

UNIT-I (9)

Amplitude Modulation: Introduction, Elements of Communication System, Amplitude Modulation, Double Sideband-Suppressed Carrier Modulation, Costas Receiver, Single-Sideband Modulation, Vestigial Sideband Modulation, Noise in Communication Systems-Sources of Noise-Shot noise, White noise, Band-Pass Receiver Structures-Super Heterodyne receiver-Intermediate frequency-AGC, delayed AGC, Noise in AM, Noise in DSB-SC, Noise in SSB-SC.

UNIT-II (9)

Angle Modulation: Basic Definitions-Frequency Modulation-Phase Modulation, Relationship between PM and FM Waves, Narrow-Band Frequency Modulation, Wide-Band Frequency Modulation, Transmission Bandwidth of FM Waves, Generation of FM Waves, Demodulation of FM Signals-Phase discriminator, Phase Locked Loop, Noise in FM-Threshold effect, Pre-emphasis and De-emphasis.

Pulse Modulation: Transition from Analog to Digital Communications, Sampling Process, Pulse-Amplitude Modulation, Pulse-Position Modulation.

UNIT-III (9)

Digital Modulation: Elements of Digital communication system, Source coding, Discrete Memoryless Source (DMS), Measure of Information, Entropy, Information Rate, Source coding- Shannon Fano, Huffman Coding, Gaussian Channel capacity - Shannon bound, Pulse-Code Modulation (PCM), Quantization, Quantization error, Signal to quantization noise ratio, Delta modulation (DM), Adaptive Delta Modulation (ADM), Comparison of PCM and DM

Baseband Data Transmission: Baseband Transmission of Digital Data, Inter Symbol Interference, Nyquist Channel, Raised-Cosine Pulse Spectrum, Baseband Transmission of M-ary Data, Eye Pattern, Equalization - Transversal Equalizer

UNIT - IV (9)

Band-pass Data Transmission: Band Pass Data transmission system, Gram Schmidt Orthogonalization Procedure, Geometric Interpretation of signals, Optimum receiver for Binary digital modulation schemes, Coherent Binary Phase Shift Keying (BPSK), Differential Phase Shift Keying (DPSK), Coherent Binary

U18EC503 COMMUNICATION SYSTEMS

Class: B.Tech. V – Semester
Engineering(ECE)

Branch: Electronics and Communication

Teaching Scheme:

L	T	P	C
3	-	-	3

Examination Scheme:

Continuous Internal Evaluation	40 marks
End Semester Examination	60 marks

Course Learning Objectives (LOs):

This course will develop students' knowledge on /in...

LO1: linear modulation strategies that constitute the amplitude modulation

LO2: angle modulation & pulse modulation

LO3: source coding, digital modulation techniques & baseband data transmission systems

LO4: bandpass data transmission systems & channel coding techniques

UNIT-I (9)

Amplitude Modulation: Introduction, Elements of Communication System, Amplitude Modulation, Double Sideband-Suppressed Carrier Modulation, Costas Receiver, Single-Sideband Modulation, Vestigial Sideband Modulation, Noise in Communication Systems-Sources of Noise-Shot noise, White noise, Band-Pass Receiver-Structures-Super Heterodyne Receiver-Intermediate frequency-AGC, Noise in AM, Noise in DSB-SC, Noise in SSB-SC.

UNIT-II (9)

Angle Modulation: Basic Definitions-Frequency Modulation-Phase Modulation, Relationship between PM and FM Waves, Narrow-Band Frequency Modulation, Wide-Band Frequency Modulation, Transmission Bandwidth of FM Waves, Generation of FM Waves, Demodulation of FM Signals-Phase discriminator, Phase Locked Loop, Noise in FM, Pre-emphasis and De-emphasis.

Pulse Modulation: Transition from Analog to Digital Communications, Sampling Process, Pulse-Amplitude Modulation, Pulse-Position Modulation.

UNIT-III (9)

Digital Modulation: Elements of Digital communication system, Source coding, Discrete Memoryless Source (DMS), Measure of Information, Entropy, Information Rate, Source coding- Shannon Fano, Huffman Coding, Gaussian Channel capacity - Shannon bound, Pulse-Code Modulation (PCM), Quantization, Quantization error, Signal to quantization noise ratio, Delta modulation (DM), Adaptive Delta Modulation (ADM), Comparison of PCM and DM

Baseband Data Transmission(Introduction): Inter Symbol Interference, Pulse shaping, Eye Pattern, Equalization

KAKATIYA INSTITUTE OF TECHNOLOGY & SCIENCE: WARANGAL-15
DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

Date: 09.02.2022

Submitted to the Principal


Sub: Modification of Syllabus- U18EC605 VLSI CIRCUITS AND SYSTEMS


It is to bring your notice that 4th unit is replaced with Verilog HDL and unnecessary content in the sequence of flow removed and necessary content to be taught is added during modification, without changing the total teaching contact hours.


This is for your favour of information and necessary initiation.

Pl. find as attachment the modified syllabus of U18EC605 VLSI CIRCUITS AND SYSTEMS, we are attaching old and new syllabus for your reference.

Thank you sir


Dr. T. Sunil Kumar
Asst. Prof., Dept. of ECE
CC Member


Dr. Ch. Sridevi
Asst. Prof., Dept. of ECE
CC Member


Mr. Ch. Pavan Kumar
Asst. Prof., Dept. of ECE
Course Coordinator

U18EC605 VLSI CIRCUITS AND SYSTEMS

Class: B.Tech.VI – Semester

Branch: Electronics and Communication Engineering (ECE)

Teaching Scheme:

L	T	P	C
3	–	–	3

Examination Scheme:

Continuous Internal Evaluation	40 marks
End Semester Examination	60 marks

Course Learning Objectives(LOs):

This course will develop students' knowledge in/on...

LO1: *fabrication process and electrical properties of MOS transistors*

LO2: *stick diagrams, design rules, layout diagrams and basic circuit concepts of MOS transistors*

LO3: *data path subsystems using structured design principles*

LO4: *basic concepts of Verilog and description of various levels of abstraction*

UNIT-I (9)

Introduction to MOS Technology: Introduction to VLSI, Basic MOS transistor, Process steps in fabricating MOSFET, Fabrication process of nMOS, CMOS and BiCMOS transistors

Basic Electrical Properties of MOS Transistor: Drain to source current and voltage relation, Threshold voltage, Transconductance, Pass transistor, nMOS inverter, Pull up/Pull down ratios, Alternate forms of pull up, CMOS inverter, BiCMOS inverter, Latch-up in CMOS circuits

UNIT - II (9)

MOS Circuit Design Processes: MOS layers, Stick diagrams - nMOS design style and CMOS design style, Lambda based design rules and Layout diagrams

Basic Circuit Concepts: Sheet resistance, Area capacitances of layers, Delay unit, Inverter delays, Rise time and Fall time estimation

UNIT - III (9)

Data path Subsystems: Introduction, Addition/Subtraction, One/Zero Detectors, Comparators, Counters, Boolean logical operations, Coding, Shifters, Multiplication, Division and Parallel-prefix computations

Subsystem Design and Layout: Architectural Issues, Switch Logic, Gate Logic, Examples of Structured Design, Clocked Sequential Circuits and System Considerations

UNIT - IV (9)

Verilog HDL: Hierarchical Modeling Concepts, Basic concepts - Data types, Modules and ports, Gate level modeling, Dataflow modeling, Behavioral modeling, Design examples of Combinational and Sequential circuits, Switch level modeling, Tasks and Functions

Text Books:

- [1] Neil H. E. Weste, David Harris and Ayan Banerjee, *CMOS VLSI Design – A Circuits and Systems Perspective*, 3rd ed., New Delhi: Pearson Education, 2005. (Chapters 1 to 4, 8,9)
- [2] Douglas A Pucknell and Kamran Eshraghian, *Basic VLSI Design*, 3rd ed., New Delhi: PHI, 2008. (Chapters 1 to 6)
- [3] Samir Palnitkar, Peter Flake, *Verilog HDL –Guide to Digital Design and Synthesis*, Pearson Education, 3rd Edition, 2003. (PART-I: Chapters 2 to 8)

Reference Books:

- [1] John P Uyemura, *Chip Design for Submicron VLSI: CMOS Layout and Simulation*, 2nd ed., Thomson /Nelson, 2010

Course Learning Outcomes (COs):

On completion of this course, students will be able to...

CO1: discuss the concepts of oxidation, photolithography & deposition techniques used in the fabrication process and assess the basic electrical properties of MOS transistors

CO2: construct the stick diagrams & mask layouts using design rules and estimate the sheet resistance, area capacitances of layers & time delays of MOS transistors

CO3: build the data path subsystems using structured design principles

CO4: develop Verilog programs for digital circuits using behavioral, dataflow, gate and switch levels of abstraction

Course Articulation Matrix (CAM):U18EC605 VLSI CIRCUITS AND SYSTEMS

CO	PO1	PO2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PO 12	PS O1	PS O2
CO1 U18EC605.1	2	2	1	1	--	1	1	1	1	1		1	2	2
CO2 U18EC605.2	2	2	1	1	--	1	1	1	1	1		1	2	2
CO3 U18EC605.3	2	2	1	1	--	1	1	1	1	1		1	2	2
CO4 U18EC605.4	2	1	1	1	1	1	1	1	1	1		1	2	2
U18EC605	2	1.75	1	1	1	1	1	1	1	1		1	2	2

KAKATIYA INSTITUTE OF TECHNOLOGY & SCIENCE:WARANGAL-15
DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

Date: 13.06.2020

CIRCULAR

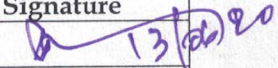
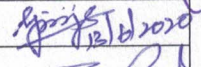

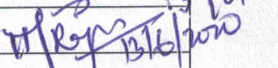
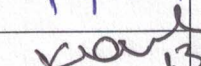
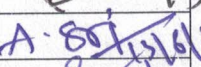
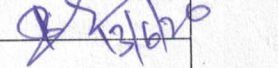
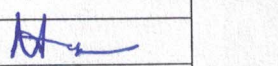
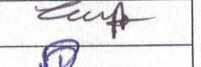




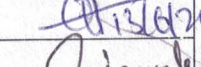
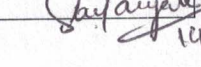



The faculty members are requested to go through the following circulars related to departmental activities completed till now.(Enclosed to this circular).

A. Circulars related to Electronics Communication and Instrumentation (ECI) course:

1. Revised Action plan for finalizing the syllabi of B.Tech-II year (III & IV semesters of ECI branch.
2. Prepare effective CO's inline with PO's and PSO's (check for reference copy of Mini project prepared by principal sir)
3. Minutes of the Meeting (MoM) of ECI virtual BoS meeting on 06.06.2020.
4. Minutes of the Meeting (MoM) of ECI virtual SSPC meeting on 09.06.2020.
5. Final draft of ECI scheme.
6. CCPC committees for B.Tech ECI-II year (III & IV semesters).

B. Circulars related to Electronics and Communication Engineering (ECE) course:

1. Revised Action plan for finalizing the syllabi of B.Tech-III year (V & VI semesters) of ECE branch.
2. Minutes of the Meeting (MoM) of Virtual Internal BoS of ECE held on 30.05.2020.
3. Final draft scheme of B.Tech ECE.
4. Syllabus of URR18 B.Tech.(ECE), V and VI semesters.
5. Virtual External BoS meeting of B.tech (ECE) scheduled on 14.06.2020 at 10.30am. ✓
6. MoU for Center of Excellence (CoE)- BLACKBUCK.

S.No.	Faculty Name	Designation	Signature
1	Dr.G.Raghotham Reddy	Professor	
2	Smt. S.P. Girija	Assoc. Professor	
3	Sri E. Suresh	Assoc. Professor	
4	Smt. A. Vijaya	Assoc. Professor	
5	Dr. M.Raju	Assoc. Professor	
6	Dr.V. Venkateshwar Reddy	Assoc. Professor	
7	Sri B. Komuraiah	Asst. Professor	
8	Sri A. Srinivas	Asst. Professor	
9	Sri K. Ramudu	Asst. Professor	
10	Mr. Syed Zaheeruddin	Asst. Professor	
11	Sri B.Narasimha	Asst. Professor	
12	Sri P.Chiranjeevi	Asst. Professor	
13	Sri V. Raju	Asst. Professor	
14	Sri D. Venu	Asst. Professor	
15	Sri R. Srikanth	Asst. Professor	
16	Dr. M. Chandrasekhar	Asst. Professor	
17	Sri S. Pradeep Kumar	Asst. Professor	
18	Sri J. SheshagiriBabu	Asst. Professor	
19	Sri A.Pavan	Asst. Professor	
20	Dr.K.Soujanya	Asst. Professor	

13/06/2020
14/06/2020
15/06/2020

21	Dr. B. Dhanalaxmi	Asst. Professor	B. d. 13/6/20
22	Sri P. Yugander	Asst. Professor	P. Y. 13/6/20
23	Sri Ch. Pavan Kumar	Asst. Professor	Ch. P. 13/6/20
24	Smt. E. Susmitha	Asst. Professor	E. S. 13/6/20
25	Mr. Md. Abdul Muqueem	Asst. Professor	M. M. 13/6/20
26	Sri V. Shobhan Reddy	Asst. Professor	V. S. 13/6/20
27	Sri G. Kranthi Kumar	Asst. Professor	G. K. 13-6-20
28	Sri D. Santhosh Kumar	Asst. Professor	D. S. 13/6/20
29	Sri D. Srinivas Rao	Asst. Professor	D. S. 13/6/20

[Signature]
Head, Dept. of ECE

KAKATIYA INSTITUTE OF TECHNOLOGY & SCIENCE: WARANGAL-15
DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

No: Covid 19/36/ECE/KITS/2020

Date: 10.06.2020

Submitted to the Principal:

Sub: Formation of Course Content Preparation Committee (CCPC) B.Tech ECI II Year
(3rd & 4th semester) URR - 18 - Reg.

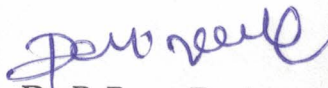
Ref: No. 36/OP/KITS/2020 dated on 20.01.2020.

With reference to the above cited, the following committees are formed to prepare the course content of B.Tech ECI II Year (3rd & 4th semester) of URR-18 scheme. The preparation of the draft course content by the respective CCPC (including Course Code, Semester, Content of 4-units, Text Books, Reference Books, Manuals for Lab courses, Course worksheet, Course Learning Objectives (LOs), Course Outcomes (COs), Course Articulation Matrix(CAM)) is to be submitted on or before 15.06.2020.

Course Content Preparation Committee (CCPC)	Course Assigned
Dr.B.Rama Devi, Chairman Prof. G. Ragotham Reddy, Convener Smt S.P. Girija, Member Dr K Sivani, Member Sri B Jeevan, Member	U18OE303E: Microprocessors U18OE311E: Microprocessors Lab U18CI406: Microprocessors Microcontrollers and Interfacing
Dr.B.Rama Devi, Chairman Smt A. Vijaya, Convener Sri D. Venu, Member Dr. K. Venu Madhav, Member Dr. K. Srinivas, Member	U18CI304: Signals Systems and Random Processes
Dr.B.Rama Devi, Chairman M.Raju, Convener E.Suresh, Member Prof. M. Sreelatha, Member Sri B. Krishna Sandeep, Member	U18CI408: Analog Circuits Laboratory
Dr.B.Rama Devi, Chairman Sri M Raghuram, Convener Sri B Shashikanth, Member Sri B. Venu Maheshwar Rao, Member	U18CI306: Measurements and Sensors U18CI308: Measurements and sensors Laboratory
Dr.B.Rama Devi, Chairman Dr.V.Venkateshwar Reddy, Convener Sri A.Srinivas, Member Dr.M.Chandrasekhar, Member Dr K Srinivas, Member Smt B Smitha, Member	U18CI403: Fundamentals of EMTL & AWP
Dr.B.Rama Devi, Chairman Sri B. Narsimha, Convener Sri R. Srikanth, Member Smt R Nirmala Devi, Sri B Shashikanth, Member	U18CI405: Signal Processing and Applications U18CI409: Signal Processing and Applications Laboratory
Dr.B.Rama Devi, Chairman Sri K. Ramudu, Convener Sri Rajashekar Thotha(industrial Expert) Prof. Shankar, Member (special Invited) Dr. K. Venu Madhav, Member	U18CI407: Programming with Python Laboratory

Terms of reference for the CCPC:

1. Preparation of Course Learning Objectives (LOs)
2. Preparation of Course Outcomes (COs)
3. Identification of Text Books/Reference Books
4. Finalization of Course Content
5. Preparation of Course Articulation Matrix (CAM)
6. Teaching Schedule (with period wise topics)


Dr. B. Rama Devi
Head, Dept. of ECE

No. /OP/KITS/2020

Date: 24/05/2020

CIRCULAR

Revised Action Plan for Finalizing the Scheme (for all semesters) & Syllabi of B.Tech - II year (III & IV semesters) of CSN & ECI branches under URR-18 scheme

S. No.	Action	Due (on or before)
1.	<u>Conduction of First Joint meeting of SSPC-CSN & SSPC-ECI:</u> <u>Agenda:</u> <ul style="list-style-type: none"> Finalization of the draft Scheme (for all semesters) of B.Tech. (CSN) & B.Tech. (ECI) branches under URR-18 scheme Guidelines for draft scheme preparation & draft course content preparation To contact external BoS members and inform in advance about the proposed virtual BoS meeting as per item detailed at S.No. 3 Adopting Programme Outcomes (POs) of NBA Formulation of Programme Specific Outcomes (PSOs) Dean AA is requested to prepare MoM in detail, with Resolutions of Joint SSPC meeting 	31.05.2020 (Sun)
2.	<u>Mail Communication to External / Internal BoS Members of CSN & ECI:</u> <ul style="list-style-type: none"> To mail the agenda of proposed First Virtual BoS meeting (by concerned HoD) 	31.05.2020 (Sun)
3.	<u>Conduction of First Virtual BoS meeting of BoS-CSN & BoS-ECI:</u> <u>Agenda:</u> <ul style="list-style-type: none"> Finalization of courses for B.Tech. (CSN) & B.Tech. (ECI) programmes Seek inputs from external BoS members on the essential content to be included in finalised courses along with appropriate standard text and reference books Adapting Programme Outcomes (POs) of NBA Approval of Formulated Programme Specific Outcomes (PSOs) To inform and request BoS members about the proposed second virtual BoS meeting as per item detailed at S.No. 11 <p>* HoDs of CSN & ECI are requested to prepare MoMs in detail, with final copy including Suggestions by External BoS Members & Resolutions of First virtual BoS meeting</p>	06.06.2020 (Sat)
4.	<u>Conduction of second Joint meeting of SSPC-CSN & SSPC-ECI:</u> <u>Agenda:</u> <ul style="list-style-type: none"> Presentation by concerned HoDs on BoS approved Schemes of B.Tech. (CSN) & B.Tech. (ECI) Discussion on suggestions given by external BoS members 	08.06.2020 (Mon)
5.	<u>Mail Communication to External BoS Members of CSN & ECI:</u> <ul style="list-style-type: none"> Finalized scheme of B.Tech. (CSN) & B.Tech. (ECI) under URR-18 to be submitted to External Members (by concerned HoD) 	09.06.2020 (Tue)

S. No.	Action	Due (on or before)
11.	<p><u>Conduction of Second Virtual BoS meeting of BoS-CSN & BoS-ECI:</u></p> <p><u>Agenda:</u></p> <ul style="list-style-type: none"> Approval of syllabi of all courses of III & IV semesters for B.Tech. (CSN) & B.Tech. (ECI) programmes Request external BoS members to acknowledge the approval of finalised syllabi through email to concerned HoD <p><i>* HoDs of CSN & ECI are requested to prepare MoMs in detail, with final copy including Suggestions by External BoS Members & Resolutions of Second virtual BoS meeting</i></p>	20.06.2020 (Sat)
12.	<p><u>Submission of BoS approved copy of syllabi of B.Tech III sem & IV sem courses & MoMs of CSN & ECI branches to Principal's office:</u></p> <p>BoS approved copy (including the approval acknowledgement emails from external BoS members) of complete syllabi under URR-18 of B.Tech III sem & IV sem courses of ECI & CSN branches along with final copy of MoM are to be mailed to principal@kitsw.ac.in</p> <p><i>(including - Course Code, Semester, content of 4-units, Text Books, Reference Books, Manuals for Lab courses, Course Worksheet, Course Learning Objectives (LOs), Course Outcomes (COs), CAM)</i></p> <p><i>(A copy to be mailed to deanaa@kitsw.ac.in)</i></p> <p><i>(Soft copy to be saved in the following format: URR18_DeptName_BranchName_3&4sem_BoSApproved_ModifiedDate Ex: URR18_CSE_CSN_3&4sem_BosApproved_24June2020)</i></p>	23.06.2020 (Tue)
13.	<p><u>Mail Communication to External / Internal AC Members:</u></p> <ul style="list-style-type: none"> To mail the agenda of proposed Virtual AC meeting <i>(by Dean AA)</i> 	24.06.2020 (Wed)
14.	<p><u>Conduction of Virtual AC Meeting:</u></p> <ul style="list-style-type: none"> To approve the syllabi of B.Tech III sem & IV sem courses of CSN & ECI branches To approve the syllabi of B.Tech V sem & VI sem courses of all branches (other than CSN & ECI) under URR-18 Dean AA is requested to prepare MoM in detail, with Resolutions of virtual AC meeting 	04.07.2020 (Sat)

Sd/-
PRINCIPAL

To
HoDs.of CSE & ECE

Copy to: 1. Secretary & Correspondent
2. All Deans
3. Members of SSPC-ECI & SSPC CSN

VISION AND MISSION OF THE INSTITUTE

Vision:

- To make our students technologically superior and ethically strong by providing quality education with the help of our dedicated faculty and staff and thus improve the quality of human life

Mission:

- To provide latest technical knowledge, analytical and practical skills, managerial competence and interactive abilities to students, so that their employability is enhanced.
- To provide a strong human resource base for catering to the changing needs of the Industry and Commerce.
- To inculcate a sense of brotherhood and national integrity.

VISION AND MISSION OF THE DEPARTMENT (ECE)

Vision:

- Develop the department into a full-fledged center of learning in various fields of Electronics and Communication Engineering in pursuit of excellence in Education, Research, Entrepreneurship and Technological services to the society

Mission:

- Imparting quality education to develop innovative and entrepreneurial professionals fit for globally competitive environment
- To nurture the students in the field of Electronics and Communication Engineering with an overall back-ground suitable for attaining a successful career in higher education, research and industry

Program Educational Objectives (PEOs)

The PEO's of the B.Tech (Electronics and Communication Engineering) program are focused on making our graduates technologically superior and ethically strong

PEO-I: Building on fundamental knowledge, graduate should continue develop technical skills within and across disciplines in Electronics and Communication Engineering for productive and successful career maintaining professional ethics

PEO-II: Graduates should develop and exercise their capabilities to demonstrate their creativity in engineering practice and team work with increasing responsibility and leadership

PEO-III: Graduates should refine their knowledge and skills to attain professional competence through lifelong learning such as higher education, advanced degrees and professional activities

U18EC610MINI PROJECT

Class:B.Tech.VI - Semester

Branch: Electronics and Communication Engineering (ECE)

Teaching Scheme:

L	T	P	C
-	-	-	2

Examination Scheme:

Continuous Internal Evaluation	100 marks
End Semester Examination	-

Course Learning Objectives(LOs):

This course will develop students' knowledge on /in...

LO1: implementing a project independently by applying knowledge to practice

LO2: literature review and well-documented report writing

LO3: creating PPTs and effective technical presentation skills

LO4: writing technical paper in scientific journal style & format and creating video pitch

Student has to take up independent mini project on innovative ideas, innovative solutions to common problems using their knowledge relevant to courses offered in their program of study, which would supplement and complement the program assigned to each student.

Guidelines:

1. The HoD shall constitute a *Department Mini Project Evaluation Committee (DMPEC)*
2. DMPEC shall allot a faculty supervisor to each student for guiding on (i) selection of topic (ii) literature survey and work to be carried out (iii) preparing a report in proper format and (iv) effective mini project oral presentation
3. There shall be only Continuous Internal Evaluation (CIE) for mini project
4. The CIE for seminar is as follows:

Assessment	Weightage
Mini Project Supervisor Assessment	20%
Working model / process / software package / system developed	20%
Mini Project report	20%
Mini Project paper	10%
Video pitch	10%
DMPEC Assessment: Oral presentation with PPT and viva-voce	20%
Total Weightage:	100%

Note: It is mandatory for the student to appear for oral presentation and viva-voce to qualify for course evaluation

- (a) **Mini Project Topic:** The topic should be interesting and conducive to discussion. Topics may be found by looking through recent issues of peer reviewed Journals / Technical Magazines on the topics of potential interest
- (b) **Working Model:** Each student is requested to develop a working model / process / system on the chosen work and demonstrate before the DMPEC as per the dates specified by DMPEC
- (c) **Report:** Each student is required to submit a well-documented report on the chosen seminar topic as per the format specified by DMPEC
- (d) **Anti-Plagiarism Check:** The seminar report should clear plagiarism check as per the Anti-Plagiarism policy of the institute
- (e) **Presentation:** Each student should prepare PPT with informative slides and make an effective oral presentation before the DMPEC as per the schedule notified by the department

- (f) **Video Pitch:** Each student should create a pitch video, which is a video presentation on his / her mini project. Video pitch should be no longer than 5 minutes by keeping the pitch concise and to the point, which shall also include key points about his / her business idea / plan (*if any*) and social impact
- (g) The student has to register for the Mini project as supplementary examination in the following cases:
- he/she is absent for oral presentation and viva-voce
 - he/she fails to submit the report in prescribed format
 - he/she fails to fulfill the requirements of Mini project evaluation as per specified guidelines
- (h) i) The CoE shall send a list of students registered for supplementary to the HoD concerned
- ii) The DSEC, duly constituted by the HoD, shall conduct Mini project evaluation and send the award list to the CoE within the stipulated time

Course Learning Outcomes(COs):

On completion of this course, students will be able to...

CO1: *apply knowledge to practice to design & conduct experiments and utilize modern tools for developing working models / process / system leading to innovation & entrepreneurship*

CO2: *demonstrate the competencies to perform literature survey, identify gaps, analyze the problem and prepare a well-documented Mini project report*

CO3: *make an effective oral presentation through informative PPTs, showing knowledge on the subject & sensitivity towards social impact of the Mini project*

CO4: *write a "Mini project paper" in scientific journal style & format from the prepared Mini project report and create a video pitch on Mini project*

Course Articulation Matrix (CAM): U18EC610 MINI PROJECT

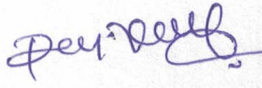


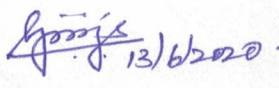


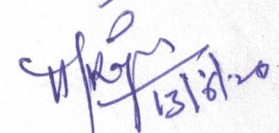
CO		PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PO 12	PSO 1	PSO 2
CO1	U18EC610.1	1	1	2	2	1	1	1	2	2	2	1	2	2	-
CO2	U18EC610.2	1	1	-	2	-	-	-	2	2	2	-	2	1	2
CO3	U18EC610.3	-	-	-	-	-	-	1	2	2	2	-	2	2	2
CO4	U18EC610.4	-	-	-	-	-	-	-	2	2	2	-	2	-	1
U18EC610		1	1	2	2	1	1	1	2	2	2	1	2	1.67	1.67

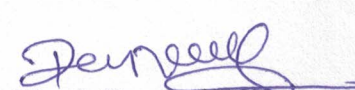
Date: 13.06.2020

CIRCULAR

This is for your kind information that virtual external BoS meeting to approve the syllabi of all courses of B.Tech(ECE) -V sem & VI sem under URR-18 is scheduled on 14.06.2020(Sunday)) at 10.30am in the Analog and Digital Simulation Laboratory B-VI-208.

BOS Members :

- | | | | |
|--|-----|-------------------------|--|
| 1. Dr. B. Rama Devi
Prof. & Head, Dept. of ECE,
KITS, Warangal | --- | Chairperson, BoS of ECE |  |
| 2. Dr. K. Ashoka Reddy
Prof. of ECE, KITS, Warangal | --- | Member |  13/06/2020 |
| 3. Dr. G.Raghotham Reddy
Prof. of ECE, KITS, Warangal | --- | Member |  13/06/20 |
| 4. Smt. S. P. Girija
Assoc. Prof. of ECE Dept. KITSW | --- | Member |  13/6/2020 |
| 5. Sri E.Suresh
Assoc. Prof. of ECE Dept. KITSW | --- | Member |  |
| 6. A.Vijaya
Assoc. Prof. of ECE Dept. KITSW | --- | Co-Opted member |  |
| 7. Dr. M. Raju
Assoc. Prof. of ECE Dept. KITSW | --- | Co-Opted member |  13/6/20 |
| 8. Dr. V.Venkateshwar Reddy
Assoc. Prof. of ECE Dept. KITSW | --- | Co-Opted member | (virtual) |


Head, Dept. of ECE

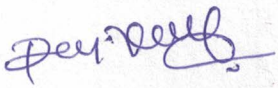


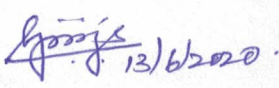


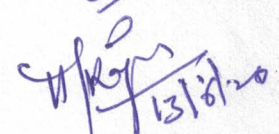
KAKATIYA INSTITUTE OF TECHNOLOGY & SCIENCE: WARANGAL-15
DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING


Date: 13.06.2020

CIRCULAR

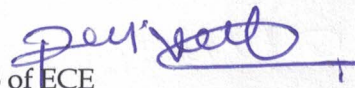

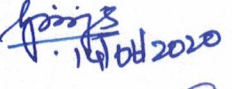




This is for your kind information that virtual external BoS meeting to approve the syllabi of all courses of B.Tech(ECE) -V sem & VI sem under URR-18 is scheduled on 14.06.2020(Sunday)) at 10.30am in the Analog and Digital Simulation Laboratory B-VI-208.

BOS Members :

- | | | | |
|--|-----|-------------------------|--|
| 1. Dr. B. Rama Devi
Prof. & Head, Dept. of ECE,
KITS, Warangal | --- | Chairperson, BoS of ECE |  |
| 2. Dr. K. Ashoka Reddy
Prof. of ECE, KITS, Warangal | --- | Member |  13/06/2020 |
| 3. Dr. G.Raghotham Reddy
Prof. of ECE, KITS, Warangal | --- | Member |  13/06/20 |
| 4. Smt. S. P. Girija
Assoc. Prof. of ECE Dept. KITSW | --- | Member |  13/6/2020 |
| 5. Sri E.Suresh
Assoc. Prof. of ECE Dept. KITSW | --- | Member |  |
| 6. A.Vijaya
Assoc. Prof. of ECE Dept. KITSW | --- | Co-Opted member |  |
| 7. Dr. M. Raju
Assoc. Prof. of ECE Dept. KITSW | --- | Co-Opted member |  13/6/20 |
| 8. Dr. V.Venkateshwar Reddy
Assoc. Prof. of ECE Dept. KITSW | --- | Co-Opted member | (virtual) |

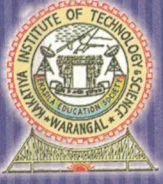

Head, Dept. of ECE

BOS Members Present

- | | | | |
|--|-----|-------------------------|--|
| 1. Dr. B. Rama Devi
Prof. & Head, Dept. of ECE,
KITS, Warangal | --- | Chairperson, BoS of ECE |  |
| 2. Dr. K. Ashoka Reddy
Prof. of ECE, KITS, Warangal | --- | Member | |
| 3. Dr. G.Raghotham Reddy
Prof. of ECE, KITS, Warangal | --- | Member |  |
| 4. Smt. S. P. Girija
Assoc. Prof. of ECE Dept. KITSW | --- | Member |  14/06/2020 |
| 5. Sri E.Suresh
Assoc. Prof. of ECE Dept. KITSW | --- | Member |  |
| 6. Sri Surya Kanth V Gangasetty
Professor, IIIT, Hyderabad | --- | External Member | |
| 7. Dr.L.Anjaneyulu
Professor & Head, Dept. of ECE, NIT,
Warangal | --- | External Member | |
| 8. Prof. T. Srinivasulu
Dean faculty of eng.
KUCE, & PRINCIPAL-UCETW
KU-Warangal | --- | External Member | |
| 9. Sri Guntha Guptha
Senior Staff Engineer Manager, Qualcomm | --- | External Member | |
| 10. Dr. Vijender Basi Reddy
Scientist, ISRO, Hyderabad | --- | External Member | |
| 11. Dr. G Sanath Kumar
Deputy Director,
Central Institute of Tool Design (CITD),
Hyderabad | --- | External Member | |
| 12. V.Madhan Kumar
Lead Physical Design Engineer,
Cerium Systems Pvt Ltd, Bangalore
Synopsis, Kondapur, Kothaguda, Hyderabad,
Telangana) (M.Tech 2009-11) | --- | External Member | |
| 13. A.Vijaya
Assoc. Prof. of ECE Dept. KITSW | --- | Co-Opted member |  |
| 14. Dr. M. Raju
Assoc. Prof. of ECE Dept. KITSW | --- | Co-Opted member |  |
| 15. Dr. V.Venkateshwar Reddy
Assoc. Prof. of ECE Dept. KITSW | --- | Co-Opted member |  |

This is for your favour of information.

Head, Dept. of ECE



Estd : 1980
KITSW

KAKATIYA INSTITUTE OF TECHNOLOGY & SCIENCE

(An Autonomous Institute under Kakatiya University, Warangal)

(Approved by AICTE, New Delhi; Recognised by UGC under 2(f) & 12(B); Sponsored by EKASILA EDUCATION SOCIETY)

Opp : Yerragattu Gutta, Hasanparthy (Mandal), WARANGAL - 506 015, Telangana, INDIA.

काकतीय प्रौद्योगिकी एवं विज्ञान संस्थान, वरंगल - ५०६ ०१५

కాకతీయ సాంకేతిక విజ్ఞాన శాస్త్ర విద్యాలయం, వరంగల్ - ५०६ ०१५

NAAC - 'A' Grade accredited Institute (CGPA : 3.21)

MHRD NIRF-2019 Rank - 180

website: www.kitsw.ac.in

e-mail: principal.kitswgl@gmail.com

☎ : +91 870 2564888

Cell : +91 73825 20585

Date: 09.06.2020

To

Prof. T. Srinivasulu,

Professor in ECE

Department of Electronics and Communication Engineering

Kakatiya University College of Engineering and Technology,

Kakatiya University, Warangal-506009, India.

Dean (Faculty of Engineering & Technology),

Kakatiya University.

Dear Sir/ Madam,

Sub: KITSW - Virtual Board of Studies meeting - Electronics and Communication Engineering - B.Tech (ECE) - Finalization of syllabi of B.Tech V Semester & VI Semester under URR18_ 14.06.2020 (Sunday) - 10.30 AM-request-Reg

Greetings !

Kakatiya Institute of Technology & Science (KITSW), Warangal is thriving continuously to provide quality education. The institute has taken up the initiative for curriculum revision of B.Tech program under URR 18 regulations in the academic year 2017-2018.

In this regard, the Department of Electronics and Communication Engineering has revised the scheme of instructions in 2018 and semester wise syllabi are being finalized every year by conducting BoS meetings periodically.

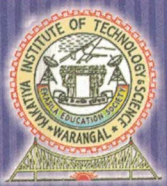
Sir, this is to bring to kind notice that syllabi of B.Tech(ECE) V & VI Semesters are to be finalized before commencement of next academic year. In view of the existing COVID-19 pandemic and the health crisis; a virtual BoS meeting is scheduled to be held tentatively on 14.06.2020 (Sunday)

You are therefore requested to kindly make it convenient to attend the Virtual Board of Studies meeting of Electronics and Communication Engineering scheduled on 14.06.2020 (Sunday) - 10.30 AM. The details of appropriate tool shall be communicated in due course.

Thank you for your continued support

Dr. B. Rama Devi
Yours sincerely,
Dr. B. Rama Devi

Dr. B. RAMA DEVI
Head of the Department (Chairperson, BoS, ECE Dept.)
Electronics & Communication Engineering
Kakatiya Institute of Technology & Science (KITSW)
WARANGAL, TELANGANA-506015



Estd : 1980
KITSW

KAKATIYA INSTITUTE OF TECHNOLOGY & SCIENCE

(An Autonomous Institute under Kakatiya University, Warangal)

(Approved by AICTE, New Delhi; Recognised by UGC under 2(f) & 12(B); Sponsored by EKASILA EDUCATION SOCIETY)

Opp : Yerragattu Gutta, Hasanparthy (Mandal), WARANGAL - 506 015, Telangana, INDIA.

काकतीय प्रौद्योगिकी एवं विज्ञान संस्थान, वरंगल - ५०६ ०१५

కాకతీయ సాంకేతిక విజ్ఞాన శాస్త్ర విద్యాలయం, వరంగల్ - ౫౦౬ ౦౧౫

NAAC - 'A' Grade accredited Institute (CGPA : 3.21)

MHRD NIRF-2019 Rank - 180

website: www.kitsw.ac.in

e-mail: principal.kitswgl@gmail.com

☎ : +91 870 2564888

Cell : +91 73825 20585

Date: 09.06.2020

To
Sri Guntha Guptha,
Senior Staff Engineer Manager, Qualcomm.

Dear Sir,

Sub: KITSW - Virtual Board of Studies meeting - Electronics and Communication Engineering - B.Tech (ECE) - Finalization of syllabi of B.Tech V Semester & VI Semester under URR18_ 14.06.2020 (Sunday) - 10.30 AM-request-Reg

Greetings !


Kakatiya Institute of Technology & Science (KITSW), Warangal is thriving continuously to provide quality education. The institute has taken up the initiative for curriculum revision of B.Tech program under URR 18 regulations in the academic year 2017-2018.

In this regard, the Department of **Electronics and Communication Engineering** has revised the scheme of instructions in 2018 and semester wise syllabi are being finalized every year by conducting BoS meetings periodically.

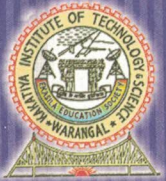
Sir, this is to bring to kind notice that syllabi of B.Tech(ECE) V & VI Semesters are to be finalized before commencement of next academic year. In view of the existing COVID-19 pandemic and the health crisis; a virtual BoS meeting is scheduled to be held tentatively on 14.06.2020 (Sunday)

You are therefore requested to kindly make it convenient to attend the Virtual Board of Studies meeting of **Electronics and Communication Engineering** scheduled on 14.06.2020 (Sunday) - 10.30 AM. The details of appropriate tool shall be communicated in due course.

Thank you for your continued support


Yours sincerely,
Dr. B. Rama Devi
(Chairperson, BoS, ECE Dept.)

Dr. B. RAMA DEVI
Head of the Department
Electronics & Communication Engineering
Kakatiya Institute of Technology & Science (KITS)
WARANGAL, TELANGANA-506015



KAKATIYA INSTITUTE OF TECHNOLOGY & SCIENCE

(An Autonomous Institute under Kakatiya University, Warangal)

(Approved by AICTE, New Delhi; Recognised by UGC under 2(f) & 12(B); Sponsored by EKASILA EDUCATION SOCIETY)

Opp : Yerragattu Gutta, Hasanparthy (Mandal), WARANGAL - 506 015, Telangana, INDIA.

Estd : 1980
KITSW

काकतीय प्रौद्योगिकी एवं विज्ञान संस्थान, वरंगल - ५०६ ०१५

కాకతీయ సాంకేతిక విజ్ఞాన శాస్త్ర విద్యాలయం, వరంగల్ - ५०६ ०१५

NAAC - 'A' Grade accredited Institute (CGPA : 3.21)

MHRD NIRF-2019 Rank - 180

website: www.kitsw.ac.in

e-mail: principal.kitswgl@gmail.com

☎ : +91 870 2564888

Cell : +91 73825 20585

Date: 09.06.2020

To
Dr. Vijender Basi Reddy,
Scientist, ISRO, Hyderabad

Dear Sir,

Sub: KITSW - Virtual Board of Studies meeting - Electronics and Communication Engineering - B.Tech (ECE) - Finalization of syllabi of B.Tech V Semester & VI Semester under URR18_ 14.06.2020 (Sunday) - 10.30 AM-request-Reg

Greetings !


Kakatiya Institute of Technology & Science (KITSW), Warangal is thriving continuously to provide quality education. The institute has taken up the initiative for curriculum revision of B.Tech program under URR 18 regulations in the academic year 2017-2018.

In this regard, the Department of Electronics and Communication Engineering has revised the scheme of instructions in 2018 and semester wise syllabi are being finalized every year by conducting BoS meetings periodically.

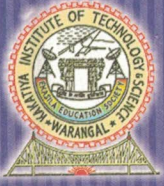
Sir, this is to bring to kind notice that syllabi of B.Tech(ECE) V & VI Semesters are to be finalized before commencement of next academic year. In view of the existing COVID-19 pandemic and the health crisis; a virtual BoS meeting is scheduled to be held tentatively on 14.06.2020 (Sunday)

You are therefore requested to kindly make it convenient to attend the Virtual Board of Studies meeting of Electronics and Communication Engineering scheduled on 14.06.2020 (Sunday) - 10.30 AM. The details of appropriate tool shall be communicated in due course.

Thank you for your continued support


Yours sincerely,
Dr. B. Rama Devi
(Chairperson, BoS, ECE Dept.)

Dr. B. RAMA DEVI
Head of the Department
Electronics & Communication Engineering
Kakatiya Institute of Technology & Science (KITS)
WARANGAL, TELANGANA-506015



Estd : 1980
KITSW

KAKATIYA INSTITUTE OF TECHNOLOGY & SCIENCE

(An Autonomous Institute under Kakatiya University, Warangal)

(Approved by AICTE, New Delhi; Recognised by UGC under 2(f) & 12(B); Sponsored by EKASILA EDUCATION SOCIETY)

Opp : Yerragattu Gutta, Hasanparthy (Mandal), WARANGAL - 506 015, Telangana, INDIA.

काकतीय प्रौद्योगिकी एवं विज्ञान संस्थान, वरंगल - ५०६ ०१५

కాకతీయ సాంకేతిక విజ్ఞాన శాస్త్ర విద్యాలయం, వరంగల్ - ౫౦౬ ౦౧౫

NAAC - 'A' Grade accredited Institute (CGPA : 3.21)

MHRD NIRF-2019 Rank - 180

website: www.kitsw.ac.in

e-mail: principal.kitswgl@gmail.com

☎ : +91 870 2564888

Cell : +91 73825 20585

Date: 09.06.2020

To
Dr. G. Sanath Kumar,
Deputy Director, Central Institute of Tool Design (CITD),
Hyderabad.

Dear Sir,

Sub: KITSW - Virtual Board of Studies meeting - Electronics and Communication Engineering - B.Tech (ECE) - Finalization of syllabi of B.Tech V Semester & VI Semester under URR18_ 14.06.2020 (Sunday) - 10.30 AM-request-Reg

Greetings !

Kakatiya Institute of Technology & Science (KITSW), Warangal is thriving continuously to provide quality education. The institute has taken up the initiative for curriculum revision of B.Tech program under URR 18 regulations in the academic year 2017-2018.

In this regard, the Department of Electronics and Communication Engineering has revised the scheme of instructions in 2018 and semester wise syllabi are being finalized every year by conducting BoS meetings periodically.

Sir, this is to bring to kind notice that syllabi of B.Tech(ECE) V & VI Semesters are to be finalized before commencement of next academic year. In view of the existing COVID-19 pandemic and the health crisis; a virtual BoS meeting is scheduled to be held tentatively on 14.06.2020 (Sunday)

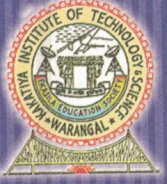
You are therefore requested to kindly make it convenient to attend the Virtual Board of Studies meeting of Electronics and Communication Engineering scheduled on 14.06.2020 (Sunday) - 10.30 AM. The details of appropriate tool shall be communicated in due course.

Thank you for your continued support


Yours sincerely,

Dr. B. Rama Devi
(Chairperson, BoS, ECE Dept.)

Dr. B. RAMA DEVI
Head of the Department
Electronics & Communication Engineering
Kakatiya Institute of Technology & Science (KITS)
WARANGAL, TELANGANA-506015



Estd : 1980
KITSW

KAKATIYA INSTITUTE OF TECHNOLOGY & SCIENCE

(An Autonomous Institute under Kakatiya University, Warangal)

(Approved by AICTE, New Delhi; Recognised by UGC under 2(f) & 12(B); Sponsored by EKASILA EDUCATION SOCIETY)

Opp : Yerragattu Gutta, Hasanparthy (Mandal), WARANGAL - 506 015, Telangana, INDIA.

काकतीय प्रौद्योगिकी एवं विज्ञान संस्थान, वरंगल - ५०६ ०१५

కాకతీయ సాంకేతిక విజ్ఞాన శాస్త్ర విద్యాలయం, వరంగల్ - ५०६ ०१५

NAAC - 'A' Grade accredited Institute (CGPA : 3.21)

MHRD NIRF-2019 Rank - 180

website: www.kitsw.ac.in

e-mail: principal.kitswgl@gmail.com

☎ : +91 870 2564888

Cell : +91 73825 20585

Date: 09.06.2020

To
Sri V.Madhan Kumar,
Lead Physical Design Engineer, Cerium Systems Pvt Ltd, Bangalore,
(Synopsys, Kondapur, Kothaguda, Hyderabad, Telangana)
(M.Tech 2009-11).

Dear Sir,

Sub: KITSW - Virtual Board of Studies meeting - Electronics and Communication Engineering - B.Tech (ECE) - Finalization of syllabi of B.Tech V Semester & VI Semester under URR18_ 14.06.2020 (Sunday) - 10.30 AM-request-Reg

Greetings !


Kakatiya Institute of Technology & Science (KITSW), Warangal is thriving continuously to provide quality education. The institute has taken up the initiative for curriculum revision of B.Tech program under URR 18 regulations in the academic year 2017-2018.

In this regard, the Department of **Electronics and Communication Engineering** has revised the scheme of instructions in 2018 and semester wise syllabi are being finalized every year by conducting BoS meetings periodically.

Sir, this is to bring to kind notice that syllabi of B.Tech(ECE) V & VI Semesters are to be finalized before commencement of next academic year. In view of the existing COVID-19 pandemic and the health crisis; a virtual BoS meeting is scheduled to be held tentatively on 14.06.2020 (Sunday)

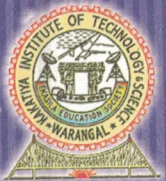
You are therefore requested to kindly make it convenient to attend the Virtual Board of Studies meeting of **Electronics and Communication Engineering** scheduled on 14.06.2020 (Sunday) - 10.30 AM. The details of appropriate tool shall be communicated in due course.

Thank you for your continued support


Yours sincerely,
Dr. B. Rama Devi

(Chairperson, BoS, ECE Dept.)

Dr. B. RAMA DEVI
Head of the Department
Electronics & Communication Engineering
Kakatiya Institute of Technology & Science (KITSW)
WARANGAL, TELANGANA-506015



Estd : 1980
KITSW

KAKATIYA INSTITUTE OF TECHNOLOGY & SCIENCE

(An Autonomous Institute under Kakatiya University, Warangal)

(Approved by AICTE, New Delhi; Recognised by UGC under 2(f) & 12(B); Sponsored by EKASILA EDUCATION SOCIETY)

Opp : Yerragattu Gutta, Hasanparthy (Mandal), WARANGAL - 506 015, Telangana, INDIA.

काकतीय प्रौद्योगिकी एवं विज्ञान संस्थान, वरंगल - ५०६ ०१५

కాకతీయ సాంకేతిక విజ్ఞాన శాస్త్ర విద్యాలయం, వరంగల్ - ५०६ ०१५

NAAC - 'A' Grade accredited Institute (CGPA : 3.21)

MHRD NIRF-2019 Rank - 180

website: www.kitsw.ac.in

e-mail: principal.kitswgl@gmail.com

☎ : +91 870 2564888

Cell : +91 73825 20585

Date: 09.06.2020

To
Sri Surya Kanth V Gangasetty,
Professor, IIIT, Hyderabad,

Dear Sir,

Sub: KITSW - Virtual Board of Studies meeting - Electronics and Communication Engineering - B.Tech (ECE) - Finalization of syllabi of B.Tech V Semester & VI Semester under URR18_ 14.06.2020 (Sunday) - 10.30 AM-request-Reg

Greetings !

Kakatiya Institute of Technology & Science (KITSW), Warangal is thriving continuously to provide quality education. The institute has taken up the initiative for curriculum revision of B.Tech program under URR 18 regulations in the academic year 2017-2018.

In this regard, the Department of Electronics and Communication Engineering has revised the scheme of instructions in 2018 and semester wise syllabi are being finalized every year by conducting BoS meetings periodically.

Sir, this is to bring to kind notice that syllabi of B.Tech(ECE) V & VI Semesters are to be finalized before commencement of next academic year. In view of the existing COVID-19 pandemic and the health crisis; a virtual BoS meeting is scheduled to be held tentatively on 14.06.2020 (Sunday)

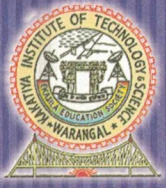
You are therefore requested to kindly make it convenient to attend the Virtual Board of Studies meeting of Electronics and Communication Engineering scheduled on 14.06.2020 (Sunday) - 10.30 AM. The details of appropriate tool shall be communicated in due course.

Thank you for your continued support


Yours sincerely,

Dr. B. Rama Devi
(Chairperson, BoS, ECE Dept.)

Dr. B. RAMA DEVI
Head of the Department
Electronics & Communication Engineering
Kakatiya Institute of Technology & Science (KITS)
WARANGAL, TELANGANA-506015



Estd : 1980
KITSW

KAKATIYA INSTITUTE OF TECHNOLOGY & SCIENCE

(An Autonomous Institute under Kakatiya University, Warangal)

(Approved by AICTE, New Delhi; Recognised by UGC under 2(f) & 12(B); Sponsored by EKASILA EDUCATION SOCIETY)

Opp : Yerragattu Gutta, Hasanparthy (Mandal), WARANGAL - 506 015, Telangana, INDIA.

కాకతీయ ప్రాధ్యోగికీ एवं विज्ञान संस्थान, వరంగల్ - 506 015

కాకతీయ సాంకేతిక విజ్ఞాన శాస్త్ర విద్యాలయం, వరంగల్ - 506 015

NAAC - 'A' Grade accredited Institute (CGPA : 3.21)

MHRD NIRF-2019 Rank - 180

website: www.kitsw.ac.in

e-mail: principal.kitswgl@gmail.com

☎ : +91 870 2564888

Cell : +91 73825 20585

Date: 09.06.2020

To
Dr.L.Anjaneyulu,
Professor & Head, Dept. of ECE,
NIT, Warangal.

Dear Sir,

Sub: KITSW - Virtual Board of Studies meeting - Electronics and Communication Engineering - B.Tech (ECE) - Finalization of syllabi of B.Tech V Semester & VI Semester under URR18_ 14.06.2020 (Sunday) - 10.30 AM-request-Reg

Greetings !

Kakatiya Institute of Technology & Science (KITSW), Warangal is thriving continuously to provide quality education. The institute has taken up the initiative for curriculum revision of B.Tech program under URR 18 regulations in the academic year 2017-2018.

In this regard, the Department of Electronics and Communication Engineering has revised the scheme of instructions in 2018 and semester wise syllabi are being finalized every year by conducting BoS meetings periodically.

Sir, this is to bring to kind notice that syllabi of B.Tech(ECE) V & VI Semesters are to be finalized before commencement of next academic year. In view of the existing COVID-19 pandemic and the health crisis; a virtual BoS meeting is scheduled to be held tentatively on 14.06.2020 (Sunday)

You are therefore requested to kindly make it convenient to attend the Virtual Board of Studies meeting of Electronics and Communication Engineering scheduled on 14.06.2020 (Sunday) - 10.30 AM. The details of appropriate tool shall be communicated in due course.

Thank you for your continued support

Yours sincerely,

Dr. B. Rama Devi
(Chairperson, BoS, ECE Dept.)

Dr. B. RAMA DEVI

Head of the Department

Electronics & Communication Engineering

Kakatiya Institute of Technology & Science (KITS)

WARANGAL, TELANGANA-506015



MoM of ECE BoS

MINUTES OF THE MEETING

OF

BOARD OF STUDIES (VIRTUAL
MEETING) HELD AT 10:30 AM ON

22.05.2021 (Saturday)

Agenda:

1. Approval of Scheme of B. Tech. VII and VIII Semesters
2. Approval of Syllabus of B. Tech. VII and VIII Semesters Courses.
3. Any other item with the permission of chair.

BoS Members Present:

S. No.	Name of the Member	Designation	Position in BoS
1.	Dr. B. Rama Devi	HoD ECE, KITSW	Chairperson, BoS
2.	Dr. K. Ashoka Reddy	Senior Professor of ECE Dept. KITSW	Member
3.	Dr. G. Raghotham Reddy	Professor of ECE Dept. KITSW	Member
4	S. P. Girija	Assoc. Prof. of ECE Dept. KITSW	Member
5.	E. Suresh	Assoc. Prof. of ECE Dept. KITSW	Member
6.	Sri Surya Kanth V Gangasetty	Professor, School of Computing K L University, Vaddeswaram - 522502, Guntur District, Andhra Pradesh	External Member (from renowned Academic Institute)
7.	Dr.L.Anjaneyulu	Professor & Head, Dept. of ECE, NIT, Warangal	External Member (from renowned Academic Institute)
8.	Prof. T. Srinivasulu	Professor in ECE Department of Electronics and Communication Engineering Kakatiya University College of Engineering and Technology, Kakatiya University, Warangal- 506009, India. Dean (Faculty of Engineering & Technology), Kakatiya University.	External Member (University Nominee)
9.	Sri Ramesh Guptha Guntha	Senior Staff Engineer Manager, Qualcomm	External Member (from Industry)
10.	Dr. Y. Jagan Mohan Reddy	Senior Engineering Manager, Honewell Technology Solutions Labs Pvt Ltd, Hyderabad	External Member (from Industry)
11.	Dr. G Sanath Kumar	Deputy Director, Central Institute of Tool Design (CITD), Hyderabad	External Member (from Industry)
12.	Sri V.Madhan Kumar	Member of technical staff, AMD India Pvt Ltd, Bangalore (M.Tech 2009-11)	External Member (Post Graduate Meritorious Alumnus – Academia/Industry)
13.	A.Vijaya	Assoc. Prof. of ECE Dept. KITSW	Co-OptedMember-1
14.	Dr. M. Raju	Assoc. Prof. of ECE Dept. KITSW	Co-OptedMember-2
15.	Dr. V.Venkateshwar Reddy	Assoc. Prof. of ECE Dept. KITSW	Co-OptedMember-3

Resolutions:

1. Virtual BoS meeting of Electronics and Communication Engineering Department was conducted on 22.05.2021, from 10:30 am to 1:00 pm through Google meet.
2. The above mentioned BoS members are present and offered their valuable suggestions.

3. BoS members of Electronics and Communication Engineering, KITSW approved

a. Scheme of B. Tech. VII and VIII Semesters

b. Syllabus of B. Tech. VII and VIII Semesters Courses & following suggestions are to be incorporate.

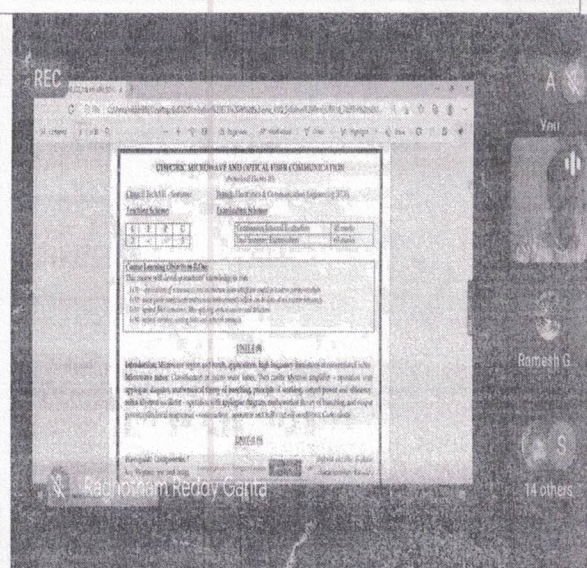
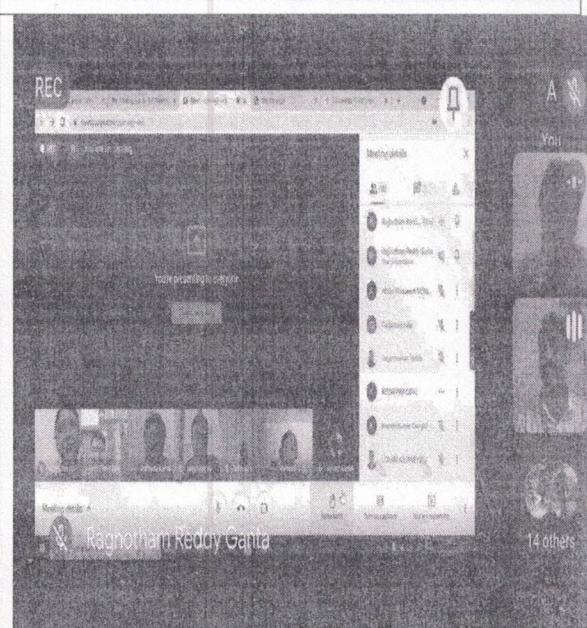
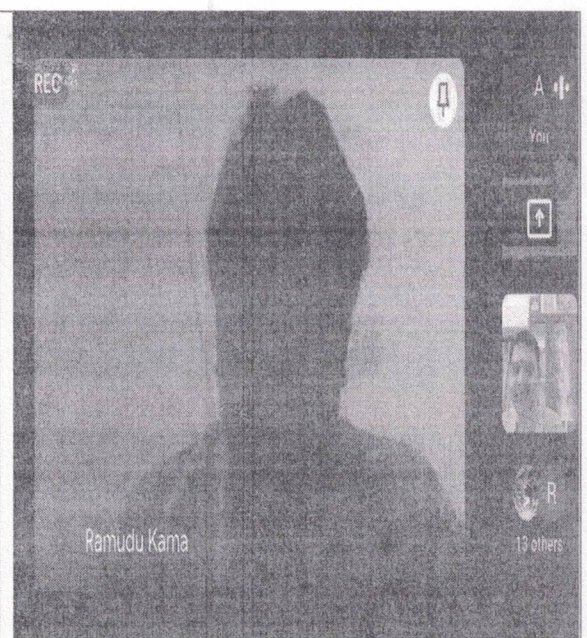
S. No.	Course Code	Course Name	Suggestions made by the BoS members	Remarks
1.	U18OE701A	Disaster Management	Unanimously approved	-
2.	U18OE701B	Project Management	Unanimously approved	-
3.	U18OE701C	Professional Ethics in Engineering	Unanimously approved	-
4.	U18OE701D	Rural Technology and Community Development	Unanimously approved	-
5.	U18EC702A	Data Science Engineering	Sanath Kumar: Natural Language Processing concepts to be included through Linux OS in unit 4.	Suggestions incorporated in the syllabus
6.	U18EC702B	Embedded Systems with RTOS and Applications	Dr.T. Srinivasulu: Modify the title	Suggestions incorporated in the syllabus
7.	U18EC702C	Microwave and Optical Fiber Communication	Syllabus Unanimously approved, as presented	-
8.	U18EC702M	MOOC course	Unanimously approved	-
9.	U18EC703A	Electronic System Design and Manufacturing	Syllabus Unanimously approved, as presented	-
10.	U18EC703B	VLSI Physical Design	Syllabus Unanimously approved, as presented	-
11.	U18EC703C	Digital Image Processing	Syllabus Unanimously approved, as presented	-
12.	U18EC703M	MOOC course	Unanimously approved	-
13.	U18EC704	Wireless Communication and Networks	Syllabus Unanimously approved, as presented	-
14.	U18EC705	Wireless Communication and Applications Lab	Dr.T. Srinivasulu: Use same name for subject and Lab Dr.Y. Jagan Mohan Reddy: 1. Use the tools like NS2, OPNET 2. Introduce experiments in WCN lab related to NS2 & OPNET	Suggestions incorporated in the syllabus
15.	U18EC706	VLSI Lab	Sanath Kumar: 1. Introduce Cadence, Matlab tools based experiments 2. Operating system changing from Windows to Linux.	Suggestions incorporated in the syllabus
16.	U18EC707	Major Project Phase – I	Unanimously approved	-
17.	U18EC708	Internship Evaluation	T. Srinivasulu: Modify the title	Suggestions incorporated in the syllabus
18.	U18EC801A	Cognitive Radio Networks	Syllabus Unanimously	

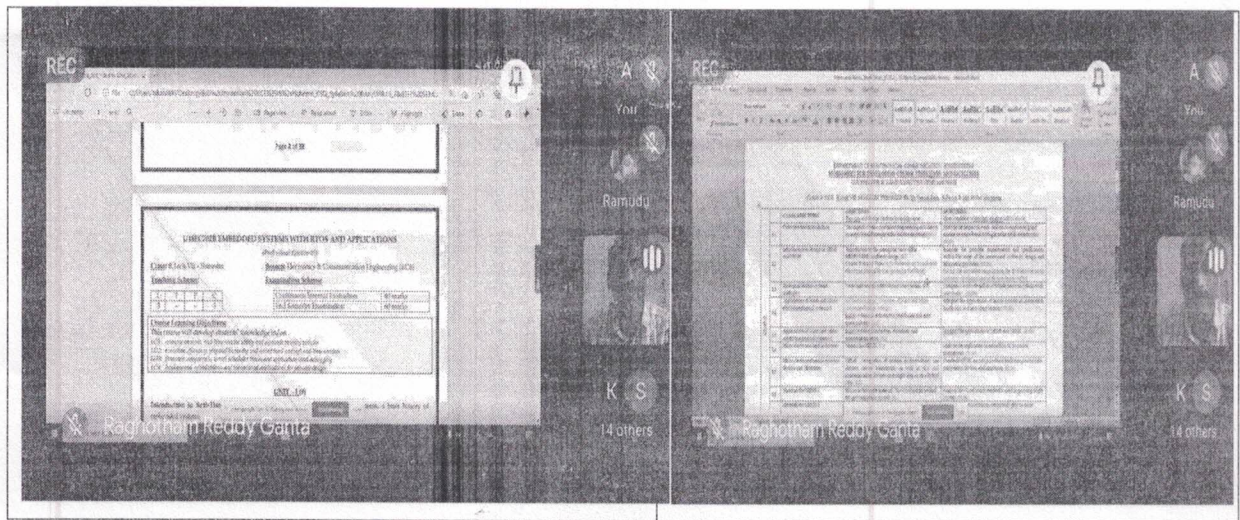
			approved, as presented	
19.	U18EC801B	FPGA-Based System Design	Sanath Kumar: 1. Introduce Zynq processor (Z-7000 series) for SoC applications, Introduction to High level Synthesis (HLS) concepts to be included in last unit	Suggestions incorporated in the syllabus
20.	U18EC801C	Radar and Satellite Communication	Dr.L.Anjaneyulu: 1. Merge radar clutter into information from radar signals 2. phased array radar concepts to be included in separate chapter	Suggestions incorporated in the syllabus
21.	U18EC801M	MOOC course	Unanimously approved	-
22.	U18EC802A	Cellular and Mobile Communication System	Ramesh Guptha Guntha: 4G and 5G concepts to be included in last unit	Suggestions incorporated in the syllabus
23.	U18EC802B	MEMs and NEMs	Syllabus Unanimously approved, as presented	-
24.	U18EC802C	Digital Speech Processing	Syllabus Unanimously approved, as presented	-
25.	U18EC802M	MOOC course	Unanimously approved	-
26.	U18OE803A	Operations Research	Unanimously approved	-
27.	U18OE803B	Management Information Systems	Unanimously approved	-
28.	U18OE803C	Entrepreneurship Development	Unanimously approved	-
29.	U18OE803D	Forex and Foreign Trade	Unanimously approved	-
30.	U18OE803M	MOOC course	Unanimously approved	-
31.	U18EC804	Major Project - Phase - II	Unanimously approved	-

Finally, Dr. B.Rama Devi, Professor & Head and Chairperson, BoS, ECE Department, thanked all the BoS members, Principal, AAC members and faculty of Electronics and Communication Engineering Department for giving their suggestions while preparing the scheme and drafting the syllabus.

Photo Gallery of Virtual BoS Meeting held on 22.05.2021 at 10.30am
through Google meet







The meeting was adjourned at 1:00pm.

Regards:

Dr. B. Rama Devi

Chairperson, BoS of ECE, KITSW





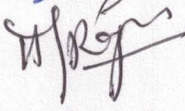
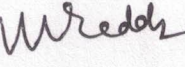
Head & Professor

Department of Electronics & Communication Engineering,

Kakatiya Institute of Technology & Science (KITSW),

Yerragattu Hillock, Bheemaram, Warangal, Telangana, India-506015.

BoS Members Present:

1.	Dr. B. Rama Devi Professor & HoD, Dept.of ECE, KITSW	---	Chairperson, BoS
2.	Dr. K. Ashoka Reddy Senior Professor, Dept.of ECE, KITSW	---	Member
3.	Dr. G. Raghotham Reddy Professor of ECE Dept. KITSW	---	Member 
4.	S. P. Girija Assoc. Prof. of ECE Dept. KITSW	---	Member 
5.	E. Suresh Assoc. Prof. of ECE Dept. KITSW	---	Member 
6.	Sri Surya Kanth V Gangasetty Professor, School of Computing K L University, Vaddeswaram - 522502, Guntur District, Andhra Pradesh	---	External Member
7.	Dr.L.Anjaneyulu Professor & Head, Dept. of ECE, NIT, Warangal	---	External Member
8.	Prof. T. Srinivasulu Professor in ECE Dept.of ECE, KUCET, KU, Warangal-506009, India.	---	External Member
9.	Sri Ramesh Guptha Guntha Senior Staff Engineer Manager, Qualcomm	---	External Member
10.	Dr. Y. Jagan Mohan Reddy Senior Engineering Manager, Honewell Technology Solutions Labs Pvt Ltd , Hyderabad	---	External Member
11.	Dr. G Sanath Kumar Deputy Director, Central Institute of Tool Design (CITD) , Hyderabad	---	External Member
12.	Sri V.Madhan Kumar Member of technical staff, AMD India Pvt Ltd , Bangalore	---	External Member
13.	A.Vijaya Assoc. Prof. of ECE Dept. KITSW	---	Co-OptedMember-1 
14.	Dr. M. Raju Assoc. Prof. of ECE Dept. KITSW	---	Co-OptedMember-2 
15.	Dr. V.Venkateshwar Reddy Assoc. Prof. of ECE Dept. KITSW	---	Co-OptedMember-3 

MoM of ECE BoS Virtual Meeting on 22.5.2021 & final scheme and Syllabus after incorporating suggestions



HOD ECE <hod.ece@kitsw.ac.in>

URR 18 B.Tech ECE VII & VIII Sem scheme & syllabus, MoM

8 messages

HOD ECE <hod.ece@kitsw.ac.in>

Mon, Jun 7, 2021 at 5:47 PM

To: Ashoka Reddy Komalla <kar.ece@kitsw.ac.in>, "grr.ece@kitsw.ac.in" <grr.ece@kitsw.ac.in>, "brd.ece@kitsw.ac.in" <brd.ece@kitsw.ac.in>, "spg.ece@kitsw.ac.in" <spg.ece@kitsw.ac.in>, "es.ece@kitsw.ac.in" <es.ece@kitsw.ac.in>, Suryakanth Gangashetty <suryakanthvgangashetty@gmail.com>, "Dr.Suryakanth V Gangashetty" <svg@kluniversity.in>, LOKAM ANJANEYULU <anjan@nitw.ac.in>, "Prof. Srinivasulu Tadisetty" <drstadisetty@gmail.com>, Ramesh Gupta Guntha <rgguntha@qti.qualcomm.com>, Jaganmohan Reddy <jreddyeturu@gmail.com>, Jaganmohan Reddy <Jeyreddy@gmail.com>, sanath@citindia.org, Madhav Kumar Vemulawada <madhavkumar1208@gmail.com>, "av.ece@kitsw.ac.in" <av.ece@kitsw.ac.in>, "mr.ece@kitsw.ac.in" <mr.ece@kitsw.ac.in>, "vvr.ece@kitsw.ac.in" <vvr.ece@kitsw.ac.in>
Cc: "kr.ece@kitsw.ac.in" <kr.ece@kitsw.ac.in>, Kranthi Kumar Gangidi <gkk.ece@kitsw.ac.in>, Office ECE <office.ece@kitsw.ac.in>

Respected BoS Members,

Greetings of the day Sir/Madam.

On behalf of management, Principal, Dept. of ECE, I personally thank all the BoS members for their wonderful support and guidance.

I am enclosing the final copies of URR 18 B.Tech ECE VII & VIII Sem scheme & syllabus with KSQ table, MoM of the BoS virtual meeting held on 22.05.2021.

I request you to approve the same. Please acknowledge the same.

Thank you.

Dr. B. Rama Devi,
Professor & HoD,
Dept. of ECE,
KITSW

Ramesh Gupta Guntha <rgguntha@qti.qualcomm.com>

Mon, Jun 7, 2021 at 5:54 PM

To: HOD ECE <hod.ece@kitsw.ac.in>, Ashoka Reddy Komalla <kar.ece@kitsw.ac.in>, "grr.ece@kitsw.ac.in" <grr.ece@kitsw.ac.in>, "brd.ece@kitsw.ac.in" <brd.ece@kitsw.ac.in>, "spg.ece@kitsw.ac.in" <spg.ece@kitsw.ac.in>, "es.ece@kitsw.ac.in" <es.ece@kitsw.ac.in>, Suryakanth Gangashetty <suryakanthvgangashetty@gmail.com>, "Dr.Suryakanth V Gangashetty" <svg@kluniversity.in>, LOKAM ANJANEYULU <anjan@nitw.ac.in>, "Prof. Srinivasulu Tadisetty" <drstadisetty@gmail.com>, Jaganmohan Reddy <jreddyeturu@gmail.com>, Jaganmohan Reddy <Jeyreddy@gmail.com>, "sanath@citindia.org" <sanath@citindia.org>, Madhav Kumar Vemulawada <madhavkumar1208@gmail.com>, "av.ece@kitsw.ac.in" <av.ece@kitsw.ac.in>, "mr.ece@kitsw.ac.in" <mr.ece@kitsw.ac.in>, "vvr.ece@kitsw.ac.in" <vvr.ece@kitsw.ac.in>
Cc: "kr.ece@kitsw.ac.in" <kr.ece@kitsw.ac.in>, Kranthi Kumar Gangidi <gkk.ece@kitsw.ac.in>, Office ECE <office.ece@kitsw.ac.in>

Hi Rama Devi,

Gone through the Syllabus documents and meeting minutes. Approved the same.

Thank you and regards

<https://mail.google.com/mail/u/0?ik=e1e50f27d8&view=pt&search=all&permthid=thread-a%3Ar-8090854946755172771&simpl=msg-a%3Ar-8095...> 1/4

Suryakanth Gangashetty <suryakanthvgangashetty@gmail.com>

Mon, Jun 7, 2021 at 6:45 PM

To: Ramesh Gupta Guntha <rgguntha@qti.qualcomm.com>

Cc: HOD ECE <hod.ece@kitsw.ac.in>, Ashoka Reddy Komalla <kar.ece@kitsw.ac.in>, "grr.ece@kitsw.ac.in" <grr.ece@kitsw.ac.in>, "brd.ece@kitsw.ac.in" <brd.ece@kitsw.ac.in>, "spg.ece@kitsw.ac.in" <spg.ece@kitsw.ac.in>, "es.ece@kitsw.ac.in" <es.ece@kitsw.ac.in>, "Dr.Suryakanth V Gangashetty" <svg@kluniversity.in>, LOKAM ANJANEYULU <anjan@nitw.ac.in>, "Prof. Srinivasulu Tadisetty" <drstadisetty@gmail.com>, Jaganmohan Reddy <jreddyeturu@gmail.com>, Jaganmohan Reddy <Jeyreddy@gmail.com>, "sanath@citdindia.org" <sanath@citdindia.org>, Madhav Kumar Vemulawada <madhavkumar1208@gmail.com>, "av.ece@kitsw.ac.in" <av.ece@kitsw.ac.in>, "mr.ece@kitsw.ac.in" <mr.ece@kitsw.ac.in>, "vvr.ece@kitsw.ac.in" <vvr.ece@kitsw.ac.in>, "kr.ece@kitsw.ac.in" <kr.ece@kitsw.ac.in>, Kranthi Kumar Gangidi <gkk.ece@kitsw.ac.in>, Office ECE <office.ece@kitsw.ac.in>

Dear All

It is fine with me.

Thank you

Yours Sincerely

Suryakanth V Gangashetty

[Quoted text hidden]

Jaganmohan Reddy <jreddyeturu@gmail.com>

Mon, Jun 7, 2021 at 8:22 PM

To: HOD ECE <hod.ece@kitsw.ac.in>

Approve.

[Quoted text hidden]

[Quoted text hidden]

[Quoted text hidden]

LOKAM ANJANEYULU <anjan@nitw.ac.in>

Mon, Jun 7, 2021 at 8:43 PM

To: HOD ECE <hod.ece@kitsw.ac.in>

The scheme and MoM are approved from my side

[Quoted text hidden]

[Quoted text hidden]

[Quoted text hidden]

--

Dr L.Anjaneyulu, SMIEEE, FIE,FIETE, LMISTE, MIAENG
Professor & Head, Dept of ECE
NIT,Warangal
Ph: 0870-2462435 , 8332969355

Prof. Srinivasulu Tadisetty <drstadisetty@gmail.com>

Tue, Jun 8, 2021 at 8:06 PM

To: Suryakanth Gangashetty <suryakanthvgangashetty@gmail.com>

Cc: Ramesh Gupta Guntha <rgguntha@qti.qualcomm.com>, HOD ECE <hod.ece@kitsw.ac.in>, Ashoka Reddy Komalla <kar.ece@kitsw.ac.in>, "grr.ece@kitsw.ac.in" <grr.ece@kitsw.ac.in>, "brd.ece@kitsw.ac.in" <brd.ece@kitsw.ac.in>, "spg.ece@kitsw.ac.in" <spg.ece@kitsw.ac.in>, "es.ece@kitsw.ac.in" <es.ece@kitsw.ac.in>, "Dr.Suryakanth V Gangashetty" <svg@kluniversity.in>, LOKAM ANJANEYULU <anjan@nitw.ac.in>, Jaganmohan Reddy

<https://mail.google.com/mail/u/0?ik=e1e50f27d8&view=pt&search=all&permthid=thread-a%3Ar-8090854946755172771&siml=msg-a%3Ar-8095...> 2/4

6/9/2021

Kakatiya Institute of Technology & Science Mail - URR 18 B.Tech ECE VII & VIII Sem scheme & syllabus, MoM

<jreddyeturu@gmail.com>, Jaganmohan Reddy <Jeyreddy@gmail.com>, "sanath@citdindia.org" <sanath@citdindia.org>, Madhav Kumar Vemulawada <madhavkumar1208@gmail.com>, "av.ece@kitsw.ac.in" <av.ece@kitsw.ac.in>, "mr.ece@kitsw.ac.in" <mr.ece@kitsw.ac.in>, "vvr.ece@kitsw.ac.in" <vvr.ece@kitsw.ac.in>, "kr.ece@kitsw.ac.in" <kr.ece@kitsw.ac.in>, Kranthi Kumar Gangidi <gkk.ece@kitsw.ac.in>, Office ECE <office.ece@kitsw.ac.in>

Prof. B. Ramadevi,

It seems okay

Regards

[Quoted text hidden]

Prof. Srinivasulu Tadisetty

B. Tech (ECE), M. Tech (E&I), Ph. D.,
LMISTE, LM ISOI, FIETE, LFBESI, SMIEEE, FLSI

Professor in ECE

Department of Electronics and Communication Engineering
Kakatiya University College of Engineering and Technology,
Kakatiya University, Warangal-506009, India

Dean (Faculty of Engineering & Technology),
Kakatiya University

G.Sanath Kumar <sanath@citdindia.org>

Wed, Jun 9, 2021 at 8:23 AM

To: Suryakanth Gangashetty <suryakanthvgangashetty@gmail.com>, "Prof. Srinivasulu Tadisetty" <drstadisetty@gmail.com>

Cc: Ramesh Gupta Guntha <rgguntha@qti.qualcomm.com>, HOD ECE <hod.ece@kitsw.ac.in>, Ashoka Reddy Komalla <kar.ece@kitsw.ac.in>, "grr.ece@kitsw.ac.in" <grr.ece@kitsw.ac.in>, "brd.ece@kitsw.ac.in" <brd.ece@kitsw.ac.in>, "spg.ece@kitsw.ac.in" <spg.ece@kitsw.ac.in>, "es.ece@kitsw.ac.in" <es.ece@kitsw.ac.in>, "Dr.Suryakanth V Gangashetty" <svg@kluniversity.in>, LOKAM ANJANEYULU <anjan@nitw.ac.in>, Jaganmohan Reddy <jreddyeturu@gmail.com>, Jaganmohan Reddy <Jeyreddy@gmail.com>, Madhav Kumar Vemulawada <madhavkumar1208@gmail.com>, "av.ece@kitsw.ac.in" <av.ece@kitsw.ac.in>, "mr.ece@kitsw.ac.in" <mr.ece@kitsw.ac.in>, "vvr.ece@kitsw.ac.in" <vvr.ece@kitsw.ac.in>, "kr.ece@kitsw.ac.in" <kr.ece@kitsw.ac.in>, Kranthi Kumar Gangidi <gkk.ece@kitsw.ac.in>, Office ECE <office.ece@kitsw.ac.in>

Dear Madam

Gone through the full syllabus and approved the same.

G sanath Kumar

Dy.Director

Get Outlook for Android

Madhan Rao <madan454@gmail.com>

Wed, Jun 9, 2021 at 2:01 PM

<https://mail.google.com/mail/u/0?ik=e1e50f27d8&view=pt&search=all&permthid=thread-a%3Ar-8090854946755172771&simpl=msg-a%3Ar-8095...> 3/4

6/9/2021

Kakatiya Institute of Technology & Science Mail - URR 18 B.Tech ECE VII & VIII Sem scheme & syllabus, MoM

To: HOD ECE <hod.ece@kitsw.ac.in>

Acknowledged and accepted the same.

Thanks & Regards,
Madan

On Wed, 9 Jun, 2021, 9:37 am HOD ECE, <hod.ece@kitsw.ac.in> wrote:

Sir,

On behalf of management, Principal, Dept. of ECE, I personally thank all the BoS members for their wonderful support and guidance.

I am enclosing the final copies of URR 18 B.Tech ECE VII & VIII Sem scheme & syllabus with KSQ table, MoM of the BoS virtual meeting held on 22.05.2021.

I request you to approve the same. Please acknowledge the same.

Dr. B. Rama Devi,
Professor & HoD,
Dept. of ECE,
KITSW

[Quoted text hidden]



DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING
KAKATIYA INSTITUTE OF TECHNOLOGY & SCIENCE:: WARANGAL – 15
(An Autonomous Institute under Kakatiya University, Warangal)

MoM of ECE BoS

MINUTES OF THE MEETING

OF

BOARD OF STUDIES (VIRTUAL
MEETING) HELD AT 10:30 AM ON

14.06.2020 (Sunday)

IN

ANALOG AND DIGITAL SIMULATION LABORATORY

OF THE DEPARTMENT

Agenda:

1. Approval of Scheme of B. Tech. V, VI, VII and VIII Semesters
2. Approval of Syllabus of B. Tech. V & VI Semesters Courses.
3. Any other item with the permission of chair.

Members Present:

S. No.	Name of the Member	Designation	Position in BoS
1.	Dr. B. Rama Devi	HoD ECE, KITSW	Chairperson, BoS
2.	Dr. K. Ashoka Reddy	Senior Professor of ECE Dept. KITSW	Member
3.	Dr. G. Raghotham Reddy	Professor of ECE Dept. KITSW	Member
4	S. P. Girija	Assoc. Prof. of ECE Dept. KITSW	Member
5.	E. Suresh	Assoc. Prof. of ECE Dept. KITSW	Member
6.	Sri Surya Kanth V Gangasetty	Professor, IIIT, Hyderabad,	External Member (from renowned Academic Institute)
7.	Dr.L.Anjaneyulu	Professor & Head, Dept. of ECE, NIT, Warangal	External Member (from renowned Academic Institute)
8.	Prof. T. Srinivasulu	Professor in ECE Department of Electronics and Communication Engineering Kakatiya University College of Engineering and Technology, Kakatiya University, Warangal-506009, India. Dean (Faculty of Engineering & Technology), Kakatiya University.	External Member (University Nominee)
9.	Sri Ramesh Guptha Guntha	Senior Staff Engineer Manager, Qualcomm	External Member (from Industry)
10.	Dr. G Sanath Kumar	Deputy Director, Central Institute of Tool Design (CITD), Hyderabad	External Member (from Industry)
11.	Sri V.Madhan Kumar	Lead Physical Design Engineer, Cerium Systems Pvt Ltd, Bangalore (Synopsys, Kondapur, Kothaguda, Hyderabad, Telangana) (M.Tech 2009-11)	External Member (Post Graduate Meritorious Alumnus – Academia/Industry)
12.	A.Vijaya	Assoc. Prof. of ECE Dept. KITSW	Co-OptedMember-1
13.	Dr. M. Raju	Assoc. Prof. of ECE Dept. KITSW	Co-OptedMember-2
14.	Dr. V.Venkateshwar Reddy	Assoc. Prof. of ECE Dept. KITSW	Co-OptedMember-3

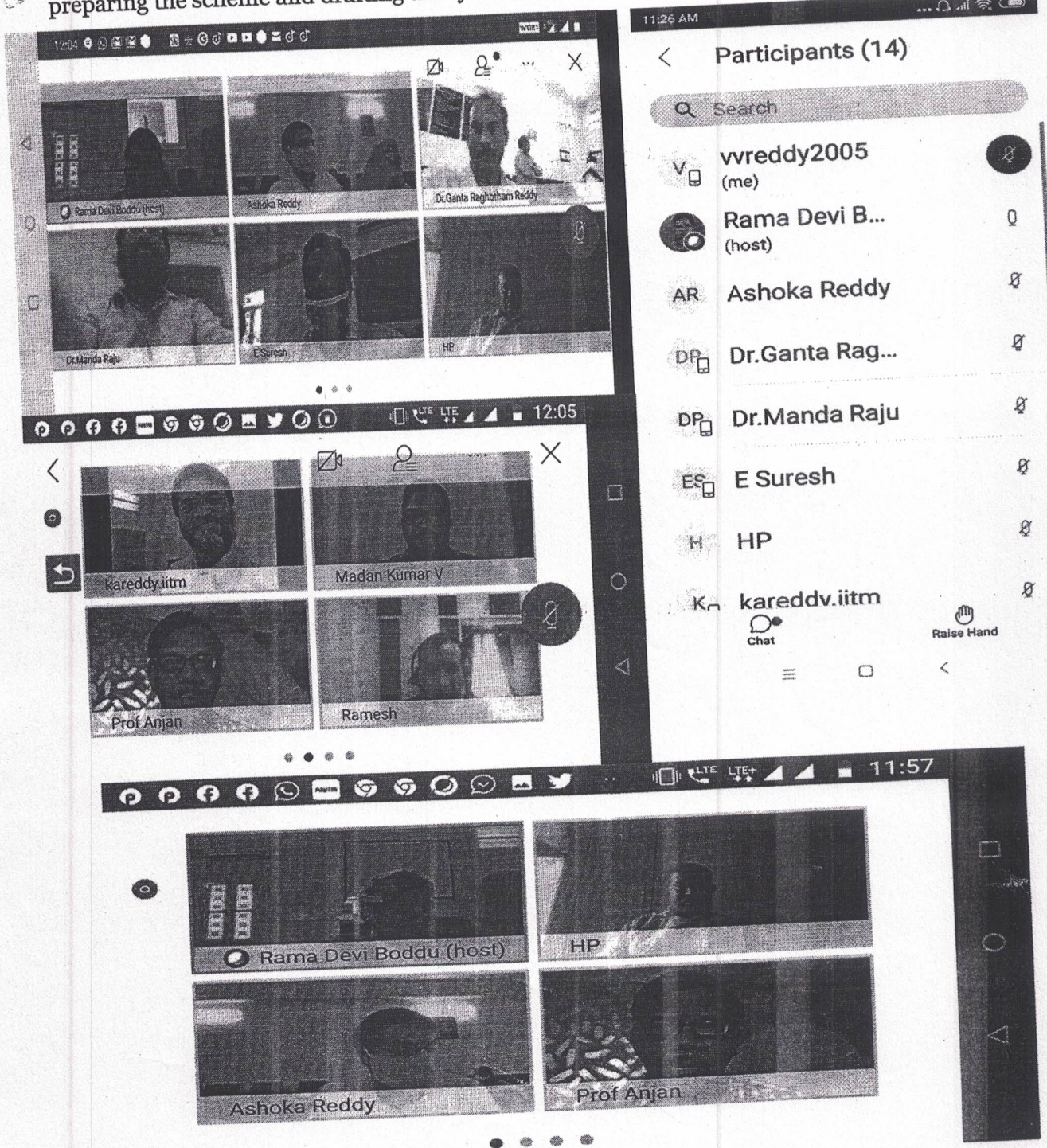
Resolutions:

1. Virtual BoS meeting of Electronics and Communication Engineering Department was conducted on 14.06.2020, from 10:30 am to 1:00 pm through Webex.
2. The above mentioned BoS members are present and offered their valuable suggestions.
3. BoS members of Electronics and Communication Engineering, KITSW approved
 - a. Scheme of B. Tech. V, VI, VII and VIII Semesters
 - b. Syllabus of B. Tech. V & VI Semesters Courses & made following suggestions to incorporate.

S. No.	Course Code	Course Name	Suggestions made by the BoS members	Remarks
1.	U18MH501	Universal Human Values -II	Syllabus Unanimously approved, as presented	
2.	U18EC502	Professional Elective - I / MOOC - I	Syllabus Unanimously approved, as presented	
3.	U18EC502A	Artificial Intelligence and Machine Learning with Python	Sanath Kumar: ML with Predictive maintenance from MATLAB tool box	Suggestions incorporated in the syllabus
4.	U18EC502B	Pervasive Computing	Syllabus Unanimously approved, as presented	
5.	U18EC502C	Electronic Measurements and Instrumentation	Syllabus Unanimously approved, as presented	
6.	U18EC502M	MOOC Course	Unanimously approved	Helps to get Honor B.Tech Degree
7.	U18EC503	Communication Systems	Syllabus Unanimously approved, as presented	
8.	U18EC504	Antennas and Wave Propagation	Syllabus Unanimously approved, as presented	
9.	U18EC505	Linear Integrated Circuits and Applications	Syllabus Unanimously approved, as presented	
10.	U18EC506	Microprocessors and Microcontrollers	Syllabus Unanimously approved, as presented.	
11.	U18EC507	Communication Systems Laboratory	Syllabus Unanimously approved, as presented	
12.	U18EC508	IC Applications Laboratory	Syllabus Unanimously approved, as presented	
13.	U18EC509	Microprocessors and Microcontrollers Laboratory	Syllabus Unanimously approved, as presented	
14.	U18EC510	Seminar	Syllabus Unanimously approved, as presented	
15.	U18TP601	Quantitative Aptitude and Logical Reasoning	Syllabus Unanimously approved, as presented	
16.	U18MH602	Management Economics and Accountancy	Syllabus Unanimously approved, as presented	
17.	U18EC603	Professional Elective -II /MOOC-II	Unanimously approved	
18.	U18EC603A	Industrial Internet of Things	Syllabus Unanimously approved, as presented	
19.	U18EC603B	Wireless Sensor Networks	Syllabus Unanimously approved, as presented	

20.	U18EC603C	Biomedical Instrumentation	Syllabus Unanimously approved, as presented	
21.	U18EC604	Digital Signal Processing and Applications	Syllabus Unanimously approved, as presented	
22.	U18EC605	VLSI Circuits and Systems	Sanath Kumar: IV-unit must be System Verilog instead of Verilog	Suggestions incorporated in the syllabus
23.	U18EC606	Embedded Systems with ARM Processor and Applications	Ramesh Guptha Guntha: Linux based ARM processor and compiler, interfacing programs to be added Madan Kumar: Linux skills are required	Syllabus is heavy. Hence, it is planned to offer Linux fundamentals in prior via internships or hands on or in CoE labs.
24.	U18EE611	Control Systems	Syllabus Unanimously approved, as presented	
25.	U18EC607	Embedded Systems and Applications laboratory	Syllabus Unanimously approved, as presented	
26.	U18EC608	Digital Signal Processing Laboratory	Syllabus Unanimously approved, as presented	
27.	U18EC610	Mini Project	Syllabus Unanimously approved, as presented	
The following suggestions to incorporate in B. Tech. VII & VIII Semester Courses				
28.	U18EC703C	FPGA based system design	Sanath Kumar: Cadence Protium S1 FPGA-Based Prototyping Platform to be included. Zynq processor concepts to be included. Madan Kumar: Tickle and Perl scripting languages Embededd with ARM processor replace with	Suggestions to be incorporated in the syllabus
29.	U18EC704	Wireless Communications and Networks	S.V.Guptha: Advanced Communication like 4G and 5G to be included	Suggestions to be incorporated in the syllabus
30.	U18EC706	VLSI Lab	V.Madhan Kumar & Sanath Kumar: Both Digital and mixed signal experiments to be covered	Suggestions to be incorporated in the syllabus
31.	U18EC802C	VLSI Physical Design	Madan Kumar: Need lab for concept for Component placement, routing, STA	Suggestions incorporated in the syllabus, better to offer in VII Sem along with U18EC706 VLSI Lab
32.	U18EC802A	Cellular and Mobile Communication System	Ramesh Guptha Guntha: Advanced mobile Communication techniques in 4G and 5G to be included T. Srinivasulu: CMC subject to be compulsory subject	Suggestions to be incorporated in the syllabus
General Suggestions:				
1.	T.Srinivasulu	1) MEMs and NEMs 2) Electronic system design and manufacturing (ESDM) These subjects are required for industry, to be included in somewhere in scheme	Suggestions will be considered while preparing the syllabus for V and VIII Semester	
2.	Sanath Kumar	RF PCB design and PCB manufacturing is highly demanded in the industry. Procure the equipment for experimentation		
3.	L.Anjaneyulu	CMOS, optimization techniques are to be included		

Finally, Dr. B. Rama Devi, Professor & Head and Chairperson, BoS, ECE Department, thanked all the BoS members, Principal, AAC members and faculty of Electronics and Communication Engineering Department for giving their suggestions while preparing the scheme and drafting the syllabus.



The meeting was adjourned at 1:00pm.

Regards:

Dr. B. Rama Devi

Chairperson, BoS of ECE, KITSW

Professor & Head,

Department of Electronics & Communication Engineering,

Kakatiya Institute of Technology & Science (KITSW),

Yerragattu Hillock, Bheemaram, Warangal, Telangana, India-506015.

BOS Members Present

- | | |
|---|--|
| 1. Dr. B. Rama Devi
Prof. & Head, Dept. of ECE,
KITS, Warangal | --- Chairperson, BoS of ECE <i>penveel</i> |
| 2. Dr. K. Ashoka Reddy
Prof. of ECE, KITS, Warangal | --- Member <i>penveel</i> |
| 3. Dr. G. Raghotham Reddy
Prof. of ECE, KITS, Warangal | --- Member <i>penveel</i> |
| 4. Smt. S. P. Girija
Assoc. Prof. of ECE Dept. KITSW | --- Member <i>penveel</i> 14/06/2020 |
| 5. Sri E. Suresh
Assoc. Prof. of ECE Dept. KITSW | --- Member <i>penveel</i> |
| 6. Sri Surya Kanth V Gangasetty
Professor, IIIT, Hyderabad | --- External Member |
| 7. Dr. L. Anjaneyulu
Professor & Head, Dept. of ECE, NIT,
Warangal | --- External Member |
| 8. Prof. T. Srinivasulu
Dean faculty of eng.
KUCE, & PRINCIPAL-UCETW
KU-Warangal | --- External Member |
| 9. Sri Guntha Guptha
Senior Staff Engineer Manager, Qualcomm | --- External Member |
| 10. Dr. G. Sanath Kumar
Deputy Director,
Central Institute of Tool Design (CITD),
Hyderabad | --- External Member |
| 11. V. Madhan Kumar
Lead Physical Design Engineer,
Cerium Systems Pvt Ltd, Bangalore
Synopsys, Kondapur, Kothaguda, Hyderabad,
Telangana) (M.Tech 2009-11) | --- External Member |
| 12. A. Vijaya
Assoc. Prof. of ECE Dept. KITSW | --- Co-Opted member <i>av</i> |
| 13. Dr. M. Raju
Assoc. Prof. of ECE Dept. KITSW | --- Co-Opted member <i>penveel</i> |
| 14. Dr. V. Venkateshwar Reddy
Assoc. Prof. of ECE Dept. KITSW | --- Co-Opted member <i>penveel</i> |

This is for your favour of information.

penveel
Head, Dept. of ECE

MoM of ECE BoS Virtual Meeting on 14.6.2020 & final scheme after incorporating suggestions

7 messages


HOD ECE <hod.ece@kitsw.ac.in>

Mon, Jun 15, 2020 at 9:53 PM

To: svg@iiit.ac.in, "Principal, KITSW" <principal@kitsw.ac.in>, "grr.ece@kitsw.ac.in" <grr.ece@kitsw.ac.in>, "spg.ece@kitsw.ac.in" <spg.ece@kitsw.ac.in>, "es.ece@kitsw.ac.in" <es.ece@kitsw.ac.in>, "mr.ece@kitsw.ac.in" <mr.ece@kitsw.ac.in>, "av.ece@kitsw.ac.in" <av.ece@kitsw.ac.in>, "vvr.ece@kitsw.ac.in" <vvr.ece@kitsw.ac.in>, suryakanthvgangashetty@gmail.com, LOKAM ANJANEYULU <anjan@nitw.ac.in>, "Prof. Srinivasulu Tadisetty" <drstadisetty@gmail.com>, Ramesh Gupta Guntha <rgguntha@qti.qualcomm.com>, citdcadcam@citdindia.org, dy.directortrg@citdindia.org, madan454@gmail.com

Respected ECE BoS members,
PFA of MoM of ECE BoS Virtual Meeting on 14.6.2020.
Enclosing the final copy of the scheme.
I request all the BoS members to acknowledge it via a reply mail.
Thank you.

Dr. B. Rama Devi,
Professor & HoD,
Dept. of ECE,
KITSW

 MoM ECE BoS Virtual Meeting and scheme modified 15.6.2020.pdf
1199K

Prof. Srinivasulu Tadisetty <drstadisetty@gmail.com>

Mon, Jun 15, 2020 at 10:29 PM

To: HOD ECE <hod.ece@kitsw.ac.in>

Madam

Is it revised SCHEMA? If so please indicate the page numbers where suggestions incorporated

Kind regards

Prof.TS

[Quoted text hidden]

[Quoted text hidden]

The content of this email is confidential and intended for the recipient specified in message only. It is strictly forbidden to share any part of this message with any third party, without a written consent of the sender. If you received this message by mistake, please reply to this message and follow with its deletion, so that we can ensure such a mistake does not occur in the future.

Prof. Srinivasulu Tadisetty

B. Tech (ECE), M. Tech (E&I), Ph. D,
LMISTE, LM ISOI, FIETE, LFBESI, SMIEEEE, FLSI

Professor in ECE

Department of Electronics and Communication Engineering
Kakatiya University College of Engineering and Technology,
Kakatiya University, Warangal-506009, India

Dean (Faculty of Engineering & Technology),
Kakatiya University

HOD ECE <hod.ece@kitsw.ac.in>

Tue, Jun 16, 2020 at 10:06 AM

To: "Prof. Srinivasulu Tadisetty" <drstadisetty@gmail.com>

Sure, will do that.

Dr. B. Rama Devi,
Professor & HoD, Dept. of ECE, KITSW

HOD ECE <hod.ece@kitsw.ac.in>

Tue, Jun 16, 2020 at 10:19 AM

To: "Prof. Srinivasulu Tadisetty" <drstadisetty@gmail.com>

SIR,

PAGE 14 & 15.


THANK YOU.

Dr. B. Rama Devi,

Professor & HoD,

Dept. of ECE,

KITSW

 Final MoM ECE BoS Virtual Meeting and scheme modified 15.6.2020.doc
1574K

LOKAM ANJANEYULU <anjan@nitw.ac.in>

Tue, Jun 16, 2020 at 11:12 AM

To: HOD ECE <hod.ece@kitsw.ac.in>

I confirm the contents of MoM

On Mon, Jun 15, 2020 at 9:53 PM HOD ECE <hod.ece@kitsw.ac.in> wrote:

--

Dr L.Anjaneyulu

Professor, Dept of ECE

NIT, Warangal

Ph: 0870-2462435 , 8332969355

Vodnala madan kumar <madan454@gmail.com>

Tue, Jun 16, 2020 at 11:43 AM

To: HOD ECE <hod.ece@kitsw.ac.in>

Cc: svg@iiit.ac.in, "Principal, KITSW" <principal@kitsw.ac.in>, "grr.ece@kitsw.ac.in" <grr.ece@kitsw.ac.in>, "spg.ece@kitsw.ac.in" <spg.ece@kitsw.ac.in>, "es.ece@kitsw.ac.in" <es.ece@kitsw.ac.in>, "mr.ece@kitsw.ac.in" <mr.ece@kitsw.ac.in>, "av.ece@kitsw.ac.in" <av.ece@kitsw.ac.in>, "vvr.ece@kitsw.ac.in" <vvr.ece@kitsw.ac.in>, suryakanthvgangashetty@gmail.com, LOKAM ANJANEYULU <anjan@nitw.ac.in>, "Prof. Srinivasulu Tadisetty" <drstadisetty@gmail.com>, Ramesh Gupta Guntha <rgguntha@qti.qualcomm.com>, citdcadcam@citdindia.org, dy.directortrg@citdindia.org

Acknowledged.

Thanks,

Madan Kumar V

9966199305

Tue, Jun 16, 2020 at 12:34 PM

SVG svg <svg@iiit.ac.in>

To: Vodnala madan kumar <madan454@gmail.com>, HOD ECE <hod.ece@kitsw.ac.in>

Cc: "Principal, KITSW" <principal@kitsw.ac.in>, "grr.ece@kitsw.ac.in" <grr.ece@kitsw.ac.in>, "spg.ece@kitsw.ac.in" <spg.ece@kitsw.ac.in>, "es.ece@kitsw.ac.in" <es.ece@kitsw.ac.in>, "mr.ece@kitsw.ac.in" <mr.ece@kitsw.ac.in>, "av.ece@kitsw.ac.in" <av.ece@kitsw.ac.in>, "vvr.ece@kitsw.ac.in" <vvr.ece@kitsw.ac.in>, "suryakanthvgangashetty@gmail.com" <suryakanthvgangashetty@gmail.com>, LOKAM ANJANEYULU <anjan@nitw.ac.in>, "Prof. Srinivasulu Tadisetty" <drstadisetty@gmail.com>, Ramesh Gupta Guntha <rgguntha@qti.qualcomm.com>, "citdcadcam@citdindia.org" <citdcadcam@citdindia.org>, "dy.directortrg@citdindia.org" <dy.directortrg@citdindia.org>

Dear Sir/Madam

Acknowledged.

Thank you

Yours Sincerely

Dr. Suryakanth V Gangashetty

IIIT Hyderabad

Ramesh Gupta Guntha

12:39 PM (0
minutes
ago)

to SVG, Vodnala, me, KITSW, grr.ece@kitsw.ac.in, spg.ece@kitsw.ac.in, es.ece@kitsw.ac.in, mr.ece@kitsw.ac.in, av.ece@kitsw.ac.in, vvr.ece@kitsw.ac.in, suryakanthvgangashetty@gmail.com, LOKAM, Srinivasulu, citdcadcam@citdindia.org, dy.directortrg@citdindia.org

Acknowledged.

Thank you and regards

Ramesh Gupta G

Venkateshwar Reddy Vedipala

to me

1:11 PM (20 minutes ago)

Respected HoD madam,

I am Dr V Venkateshwar Reddy, Associate Professor, in the department of ECE, KITSWarangal.

As per my knowledge, scheme and syllabus are good.

Acknowledged.

Thank you.

Dear Sir/Madam

Acknowledged.

Thank you

Yours Sincerely

Dr. Suryakanth V Gangashetty

IIIT Hyderabad

HOD ECE <hod.ece@kitsw.ac.in>

Tue, Jun 16, 2020 at 6:52 PM

To: svg@iiit.ac.in, "Principal, KITSW" <principal@kitsw.ac.in>, "grr.ece@kitsw.ac.in" <grr.ece@kitsw.ac.in>, "spg.ece@kitsw.ac.in" <spg.ece@kitsw.ac.in>, "es.ece@kitsw.ac.in" <es.ece@kitsw.ac.in>, "mr.ece@kitsw.ac.in" <mr.ece@kitsw.ac.in>, "av.ece@kitsw.ac.in" <av.ece@kitsw.ac.in>, "vvr.ece@kitsw.ac.in" <vvr.ece@kitsw.ac.in>, suryakanthvgangashetty@gmail.com, LOKAM ANJANEYULU <anjan@nitw.ac.in>, "Prof. Srinivasulu Tadisetty" <drstadisetty@gmail.com>, Ramesh Gupta Guntha <rgguntha@qti.qualcomm.com>, citdcadcam@citdindia.org, dy.directortrg@citdindia.org, madan454@gmail.com


Respected BoS members,


PFA of final scheme and syllabus with the modifications suggested by BoS members.


Thank you.

Dr. B. Rama Devi,
Professor & HoD,
Dept. of ECE,
KITSW

3 attachments

 Final_B.Tech ECE V Sem Syllabus 16.6.2020@3PM.doc
480K

 URR18 ECE Scheme final 15.6.2020_incorporating BoS members suggetion.doc
378K

 Final_B.Tech ECE VI sem syllabus 16.6.2020@3PM.docx
174K

Deputy director TRG - <dy.directortrg@citdindia.org>

Tue, Jun 16, 2020 at 7:10 PM

To: HOD ECE <hod.ece@kitsw.ac.in>

Dear madam

After verification of the final copy it to inform you that the syllabus is approved and can be considered.

Regards

G SANATH KUMAR

Dy.director

Prof. Srinivasulu Tadisetty

Tue, Jun 16, 10:50 PM (6 hours ago)

to me

Seems to be okay

Regards

The content of this email is confidential and intended for the recipient specified in message only. It is strictly forbidden to share any part of this message with any third party, without a written consent of the sender. If you received this message by mistake, please reply to this message and follow with its deletion, so that we can ensure such a mistake does not occur in the future.

--

Prof. Srinivasulu Tadisetty

B. Tech (ECE), M. Tech (E&I), Ph. D,
LMISTE, LM ISOL, FIETE, LFBESI, SMIEEE, FLSI

Professor in ECE

Department of Electronics and Communication Engineering
Kakatiya University College of Engineering and Technology,
Kakatiya University, Warangal-506009, India

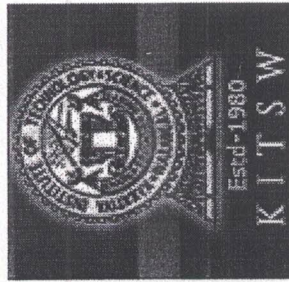
Dean (Faculty of Engineering & Technology),
Kakatiya University

URR-18

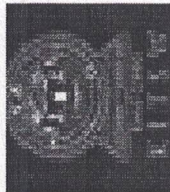
(Applicable from the Academic Year 2018-19)

**B.Tech. ELECTRONICS AND COMMUNICATION ENGINEERING (ECE)
AUTONOMOUS - REVISED SCHEME & SYLLABI (URR'18)
(w.e.f. 2018-19)
Of**

B.Tech ECE SYLLABI (I to VIII SEMESTERS)



KAKATIYA INSTITUTE OF TECHNOLOGY & SCIENCE: WARANGAL-15
(An Autonomous Institution under Kakatiya University)



KAKATIYA INSTITUTE OF TECHNOLOGY & SCIENCE: WARANGAL-15
(An Autonomous Institute under Kakatiya University, Warangal)

SCHEME OF INSTRUCTIONS & EVALUATION FOR B.TECH. 4-YEAR DEGREE PROGRAMME

BRANCH : B.Tech. - CE / EEE / ECE/ECI/CSE (AI & ML) (Stream - II)
SEMESTER : FIRST

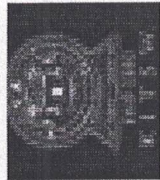
Sl.No	Course Category	Course Code	Course Name	Periods/week			Credits	Evaluation Scheme					
				L	T	P		C	CIE			ESE	Total Marks
									TA	MSE	Total		
1	BSC	U18MH101	Engineering Mathematics - I	3	1	-	4	10	30	40	60	100	
2	ESC	U18CS102	Programming for Problem Solving using C	3	-	-	3	10	30	40	60	100	
3	BSC	U18CH103	Engineering Chemistry	3	1	-	4	10	30	40	60	100	
4	ESC	U18ME104	Engineering Drawing	2	-	4	4	10	30	40	60	100	
5	ESC	U18CE105	Engineering Mechanics	3	1	-	4	10	30	40	60	100	
6	ESC	U18CS107	Programming for Problem Solving using C Laboratory	-	-	2	1	40	-	40	60	100	
7	BSC	U18CH108	Engineering Chemistry Laboratory	-	-	2	1	40	-	40	60	100	
8	MC	U18CH109	Environmental Studies*	2	-	-	-	10	30	40	60	100	
9	MC	U18EA110	EAA* : Sports/Yoga/NSS	-	-	2	-	100	-	100	-	100	
10	MC	U18EA111	Universal Human Values-I (Induction Program)	-	-	-	-	-	-	-	-	-	
Total				16	3	10	21	240	180	420	480	900	

Note: L - Lectures; T - Tutorials; P - Practicals; CIE - Continuous Internal Evaluation; TA - Teachers Assessment;

MSE - Mid Semester Examination; ESE - End Semester Examination; EAA - Extra Academic Activity;

* indicates mandatory non-credit course

Student Contact Hours / Week : 29
(periods/week) Total Credits (C) : 21 Credits



KAKATIYA INSTITUTE OF TECHNOLOGY & SCIENCE: WARANGAL-15

(An Autonomous Institute under Kakatiya University, Warangal)

SCHEME OF INSTRUCTIONS & EVALUATION FOR B.TECH. 4-YEAR DEGREE PROGRAMME

BRANCH : B.Tech. - CE / EEE / ECE/ECI/CSE (AI & ML) (Stream - II)

SEMESTER : SECOND

Sl.No	Course Category	Course Code	Course Name	Periods/week			Credits	Evaluation Scheme					
				L	T	P		C	CIE			ESE	Total Marks
									TA	MSE	Total		
1	BSC	U18MH201	Engineering Mathematics - II	3	1	-	4	10	30	40	60	100	
2	ESC	U18CS202	Data Structures through C	3	-	-	3	10	30	40	60	100	
3	BSC	U18PH203	Engineering Physics	3	1	-	4	10	30	40	60	100	
4	HSMC	U18MH204	English for Communication	2	-	2	3	10	30	40	60	100	
5	ESC	U18EE205	Basic Electrical Engineering	3	1	-	4	10	30	40	60	100	
6	ESC	U18EE206	Basic Electrical Engineering Laboratory	-	-	2	1	40	-	40	60	100	
7	ESC	U18CS207	Data Structures through C Laboratory	-	-	2	1	40	-	40	60	100	
8	BSC	U18PH208	Engineering Physics Laboratory	-	-	2	1	40	-	40	60	100	
9	ESC	U18ME209	Workshop Practice	-	-	2	1	40	-	40	60	100	
10	MC	U18EA210	EAA* : Sports/Yoga/NSS	-	-	2	-	100	-	100	-	100	
Total				14	3	12	22	310	150	460	540	1000	

Note: L - Lectures; T - Tutorials; P - Practicals; CIE - Continuous Internal Evaluation; TA - Teachers Assessment;

MSE - Mid Semester Examination; ESE - End Semester Examination; EAA - Extra Academic Activity;

* indicates mandatory non-credit course

Student Contact Hours / Week : 29
(periods/week) Total Credits (C) : 22 Credits



DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING
KAKATIYA INSTITUTE OF TECHNOLOGY & SCIENCE:: WARANGAL - 15
(An Autonomous Institute under Kakatiya University, Warangal)

SCHEME OF INSTRUCTION & EVALUATION
III SEMESTER OF 4-YEAR B.TECH ECE DEGREE PROGRAM

III - Semester [Second year] [6Th+2P+1M]

Sl. No	Category	Course Code	Course Title	Hours per week			Credits	Evaluation Scheme				
				L	T	P		CIE			ESE	Total Marks
								TA	MSE	Total		
1	BSC	U18MH301	Engineering Mathematics - III	3	1	-	4	10	30	40	60	100
2	HSMC	U18TP302	Soft and Interpersonal Skills	-	-	2	1	100	-	100	-	100
3	OE	U18OE303	Open Elective-I	3	-	-	3	10	30	40	60	100
4	PCC	U18EC304	Signals & Systems	3	-	-	3	10	30	40	60	100
5	PCC	U18EC305	Analog Circuits - I	3	-	-	3	10	30	40	60	100
6	PCC	U18EC306	Switching Theory & Logic Design	3	-	-	3	10	30	40	60	100
7	ESC	U18EE312	Network Analysis	3	-	-	2	10	30	40	60	100
8	PCC	U18EC308	Analog Circuits - I Laboratory	-	-	2	1	40	-	40	60	100
9	OE	U18OE311	Open Elective-I based Laboratory	-	-	2	1	40	-	40	60	100
Total:				18	1	6	21	240	180	420	480	900

[L= Lecture, T = Tutorials, P = Practicals & C = Credits]

Open Elective-I:

U18OE303A: Object Oriented Programming (CSE)
 U18OE303B: Fluid Mechanics & Hydraulic Machines (CE)
 U18OE303C: Fundamentals of Mechatronics (ME)
 U18OE303D: Web Programming (IT)
 U18OE303F: Strength of Materials (CE)

Open Elective-I based Laboratory

U18OE311A: Object Oriented Programming Lab (CSE)
 U18OE311B: Fluid Mechanics & Hydraulic Machines Lab (CE)
 U18OE311C: Mechatronics Lab (ME)
 U18OE311D: Web Programming Lab (IT)
 U18OE311F: Strength of Materials Lab (CE)

Student Contact Hours/ Week : 25
 (periods/week) Total Credits (C) : 21 Credits



DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING
KAKATIYA INSTITUTE OF TECHNOLOGY & SCIENCE:: WARANGAL - 15
(An Autonomous Institute under Kakatiya University, Warangal)

SCHEME OF INSTRUCTION & EVALUATION
IV SEMESTER OF 4-YEAR B.TECH ECE DEGREE PROGRAM

IV - Semester [Second year] [6Th+2P+2M]

Sl. No	Category	Course Code	Course Title	Hours per week			Credits	Evaluation Scheme				
				L	T	P		CIE			ESE	Total Marks
								TA	MSE	Total		
1	OE	U18OE401	Open Elective-II	3	1	-	4	10	30	40	60	100
2	HSMC	U18MH402	Professional English	-	-	2	1	100	-	100	-	100
3	PCC	U18EC403	Electro Magnetic Waves and Transmission Lines	3	-	-	3	10	30	40	60	100
4	PCC	U18EC404	Analog Circuits - II	3	-	-	3	10	30	40	60	100
5	PCC	U18EC405	Pulse and Digital Circuits	3	-	-	3	10	30	40	60	100
6	PCC	U18EC406	Probability and Random Processes	3	-	-	3	10	30	40	60	100
7	PCC	U18EC407	Digital Design	3	-	-	3	10	30	40	60	100
8	MC	U18MH415	Essence of Indian Traditional Knowledge	2	-	-	-	10	30	40	60	100
9	PCC	U18EC408	Analog Circuits - II Laboratory	-	-	2	1	40	-	40	60	100
10	PCC	U18EC409	Pulse and Digital Circuits Laboratory	-	-	2	1	40	-	40	60	100
				20	1	6	22	250	210	460	540	1000
11	MC	U18CH416	Environmental Studies *	2	-	-	0	10	30	40	60	100

* indicates Mandatory Non-Credit course for Lateral Entry Students Only [L= Lecture, T = Tutorials, P = Practicals & C = Credits]

Open Elective-II

U18OE401A: Applicable Mathematics (M&H)
 U18OE401C: Elements of Mech. Engg. (ME)
 U18OE401E: Computers Networks (IT)
 U18OE401F: Renewable Energy Resources (EEE)

Student Contact Hours / Week : 27
 (periods/week) Total Credits (C) : 22 Credits



DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING
KAKATIYA INSTITUTE OF TECHNOLOGY & SCIENCE:: WARANGAL - 15
(An Autonomous Institute under Kakatiya University, Warangal)

SCHEME OF INSTRUCTION & EVALUATION
V SEMESTER OF 4-YEAR B.TECH DEGREE PROGRAM

[5Th+3P+1MC]

SL. No	Category	Course Code	Course Title	Hours per week			Credits	Evaluation Scheme				
				L	T	P		CIE		ESE	Total Marks	
								TA	MSE			Total
1	MC	U18MH501	Universal Human Values - II	2	-	-	-	10	30	40	60	100
2	PE	U18EC502	Professional Elective - I / MOOC - I	3	-	-	3	10	30	40	60	100
3	PCC	U18EC503	Communication Systems	3	-	-	3	10	30	40	60	100
4	PCC	U18EC504	Antennas and Wave Propagation	3	-	-	3	10	30	40	60	100
5	PCC	U18EC505	Linear Integrated Circuits and Applications	3	-	-	3	10	30	40	60	100
6	PCC	U18EC506	Microprocessors and Microcontrollers	3	-	-	3	10	30	40	60	100
7	PCC	U18EC507	Communication Systems Laboratory	-	-	2	1	40	-	40	60	100
8	PCC	U18EC508	IC Applications Laboratory	-	-	2	1	40	-	40	60	100
9	PCC	U18EC509	Microprocessors and Microcontrollers Laboratory	-	-	2	1	40	-	40	60	100
10	PROJ	U18EC510	Seminar	-	-	2	1	100	-	100	-	100
Total:				17	-	8	19	280	180	460	540	1000

[L= Lecture, T = Tutorials, P = Practicals & C = Credits]

Professional Elective-I/MOOC - I:

U18EC502A: Artificial Intelligence and Machine Learning with Python

U18EC502B: Pervasive Computing

U18EC502C: Electronic Measurements and Instrumentation

U18EC502M: MOOC Course

Student Contact Hours / Week : 25 (periods/week)
Total Credits (C) : 19 Credits

Dr. V. Venkateshwar Reddy

Dr. V. Venkateshwar Reddy,
Assoc. Professor

S.P. Girija

S.P. Girija,
Assoc. Professor

Dr. M. Raju

Dr. M. Raju,
Assoc. Professor

Dr. G. Raghobham Reddy

Dr. G. Raghobham Reddy, Professor

Smt. A. Vijaya

Smt. A. Vijaya,
Assoc. Professor

Prof. K. Ashoka Reddy

Prof. K. Ashoka Reddy,
Principal

E. Suresh

E. Suresh,
Assoc. Professor or

Dr. B. Rama Devi

Dr. B. Rama Devi, Professor &
Head, Chairperson-BoS in ECE



DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING
KAKATIYA INSTITUTE OF TECHNOLOGY & SCIENCE:: WARANGAL - 15
(An Autonomous Institute under Kakatiya University, Warangal)
SCHEME OF INSTRUCTION & EVALUATION
VI SEMESTER OF 4-YEAR B.TECH DEGREE PROGRAM

Sl. No	Category	Course Code	Course Title	Hours per week			Credits	Evaluation Scheme				
								CIE			ESE	Total Marks
								TA	MSE	Total		
1	HSMC	U18TP601	Quantitative Aptitude & Logical Reasoning	2	-	-	1	10	30	40	60	100
2	HSMC	U18MH602	Management Economics & Accountancy	3	-	-	3	10	30	40	60	100
3	PE	U18EC603	Professional Elective -II / MOOC-II	3	-	-	3	10	30	40	60	100
4	PCC	U18EC604	Digital Signal Processing and Applications	3	-	-	3	10	30	40	60	100
5	PCC	U18EC605	VLSI Circuits and Systems	3	-	-	3	10	30	40	60	100
6	ESC	U18EE611	Control Systems	3	-	-	3	10	30	40	60	100
7	PCC	U18EC606	Embedded Systems with ARM Processor and Applications	3	-	-	3	10	30	40	60	100
8	PCC	U18EC607	Embedded Systems and Applications laboratory	-	-	2	1	40	-	40	60	100
9	PCC	U18EC608	Digital Signal Processing Laboratory	-	-	2	1	40	-	40	60	100
10	PROJ	U18EC610	Mini Project	-	-	2	1	100	-	100	-	100
Total:				20	-	6	22	250	210	460	540	1000

[L= Lecture, T = Tutorials, P = Practicals & C = Credits]

Professional Elective-II / MOOC -II:

U18EC603A: Industrial Internet of Things

U18EC603B: Wireless Sensor Networks

U18EC603C: Biomedical Instrumentation

U18EC603M: MOOC Course

Student Contact Hours / Week (periods/week) : 26

Total Credits (C) : 19 Credits

Dr. V. Venkateshwar Reddy,
Assoc. Professor

S.P. Girija,
Assoc. Professor

Dr. M. Raju,
Assoc. Professor

Dr. G. Raghotham Reddy,
Professor

Smt. A. Vijaya,
Assoc. Professor

Prof. K. Ashoka Reddy,
Principal

E. Suresh,
Assoc. Professor or

Dr. B. Rama Devi, Professor &
Head, Chairperson-BoS in ECE



DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING
KAKATIYA INSTITUTE OF TECHNOLOGY & SCIENCE:: WARANGAL - 15
(An Autonomous Institute under Kakatiya University, Warangal)
SCHEME OF INSTRUCTION & EVALUATION
VII SEMESTER OF 4-YEAR B.TECH DEGREE PROGRAM

Sl. No	Category	Course Code	Course Title	Hours per week			Credits	Evaluation Scheme				
				L	T	P		CIE			ESE	Total Marks
								TA	MSE	Total		
1	OE	U18OE701	Open Elective- III	3	-	-	3	10	30	40	60	100
2	PE	U18EC702	Professional Elective - III / MOOC-III	3	-	-	3	10	30	40	60	100
3	PE	U18EC703	Professional Elective - IV / MOOC-IV	3	-	-	3	10	30	40	60	100
4	PCC	U18EC704	Wireless Communication and Networks	3	-	-	3	10	30	40	60	100
5	PCC	U18EC705	Wireless Communication and Applications Lab	-	-	2	1	40	-	40	60	100
6	PCC	U18EC706	VLSI Lab	-	-	2	1	40	-	40	60	100
7	PROJ	U18EC707	Major Project Phase - I	-	-	6	3	100	-	100	-	100
8	MC	U18EC708	Internship Evaluation	-	-	2	-	100	-	100	-	100
Total:				12	-	12	17	320	120	440	360	800

[4Th+2P+1MC]

[[Lecture ,T = Tutorial, P = Practicals, C = Project, MC = Minor Course]]

[L = Lecture, T = Tutorials, P = Practicals & C = Credits] Systems

Open Elective-III: U18OE701A: Disaster Management U18OE701B: Project Management U18OE701C: Professional Ethics in Engineering U18OE701D: Rural Technology and Community Development	Professional Elective-III / MOOC-III: U18EC702A: Data Science and Applications U18EC702B: Embedded Systems with RTOS and Applications U18EC702C: Microwave and Optical Fiber Communication U18EC702M: MOOC course	Professional Elective-IV / MOOC-IV: U18EC703A: Electronic System Design and Manufacturing U18EC703B: VLSI Physical Design U18EC703C: Digital Image Processing U18EC703M: MOOC course
--	--	---

Student Contact Hours / Week (periods/week) : 26
Total Credits (C) : 19 Credits

Dr. V. Venkateshwar Reddy,
Assoc. Professor

S.P. Girija,
Assoc. Professor

Dr. M. Raju,
Assoc. Professor

Dr. G. Raghotham Reddy, Professor

Smt. A. Vijaya,
Assoc. Professor

Prof. K. Ashoka Reddy,
Principal

E. Suresh,
Assoc. Professor or

Dr. B. Rama Devi, Professor &
Head, Chairperson-BoS in ECE



DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING
KAKATIYA INSTITUTE OF TECHNOLOGY & SCIENCE:: WARANGAL - 15
(An Autonomous Institute under Kakatiya University, Warangal)

SCHEME OF INSTRUCTION & EVALUATION
VIII SEMESTER OF 4-YEAR B.TECH DEGREE PROGRAM

[3Th+0P+0MC]

31h+0P+0MC												
Sl. No	Category	Course Code	Course Title	Hours per week			Credits	Evaluation Scheme				
				L	T	P		CIE			ESE	Total Marks
								TA	MSE	Total		
1	PE	U18EC801	Professional Elective - V / MOOC-V	3	-	-	3	10	30	40	60	100
2	PE	U18EC802	Professional Elective - VI / MOOC-VI	3	-	-	3	10	30	40	60	100
3	OE	U18OE803	Open Elective - IV / MOOC-VII	3	-	-	3	10	30	40	60	100
4	PROJ	U18EC804	Major Project - Phase - II	-	-	14	7	40	-	40	60	100
Total:				9	-	14	16	70	90	160	240	400

[L = Lecture, T = Tutorials, P = Practicals & C = Credits]

Professional Elective-V / MOOC-V: U18EC801A: Cognitive Radio Networks U18EC801B: FPGA-Based System Design U18EC801C: Radar and Satellite Communication U18EC801M: MOOC course	Professional Elective-VI / MOOC-VI: U18EC802A: Cellular and Mobile Communication System U18EC802B: MEMs and NEMs U18EC802C: Digital Speech Processing U18EC802M: MOOC course	Open Elective-IV / MOOC-VII: U18OE803A: Operations Research U18OE803B: Management Information Systems U18OE803C: Entrepreneurship Development U18OE803D: Forex and Foreign Trade U18OE803M: MOOC course
--	--	---

Student Contact Hours / Week (periods/week) : 26
Total Credits (C) : 19 Credits

Dr. V. Venkateshwar Reddy
Dr. V. Venkateshwar Reddy,
Assoc. Professor

S.P. Girija
S.P. Girija,
Assoc. Professor

Dr. M. Raju
Dr. M. Raju,
Assoc. Professor

Dr. G. Raghotham Reddy
Dr. G. Raghotham Reddy, Professor

Smt. A. Vijaya
Smt. A. Vijaya,
Assoc. Professor

Prof. K. Ashoka Reddy
Prof. K. Ashoka Reddy,
Principal

E. Suresh
E. Suresh,
Assoc. Professor or


Dr. B. Rama Devi
Dr. B. Rama Devi, Professor &
Head, Chairperson-BoS in ECE





DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING
KAKATIYA INSTITUTE OF TECHNOLOGY & SCIENCE:: WARANGAL - 15
(An Autonomous Institute under Kakatiya University, Warangal)


SEMESTER WISE CREDITS
DISTRIBUTION


SEM	No. of Credits	Contact hours
I	21	29
II	22	29
III	21	25
IV	22	27
V	19	25
VI	22	26
VII	17	24
VIII	16	23
Total	160	208



Dr. V. Venkateshwar Reddy,
Assoc. Professor



S.P. Girija,
Assoc. Professor



Dr. M. Raju,
Assoc. Professor


Dr. G. Raghatham
Reddy, Professor


Smt. A. Vijaya,
Assoc. Professor


Prof. K. Ashoka Reddy,
Principal


E. Suresh,
Assoc. Profess or


Dr. B. Rama Devi, Professor &
Head, Chairperson-BoS in ECE



DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

KAKATIYA INSTITUTE OF TECHNOLOGY & SCIENCE: WARANGAL-15

(An Autonomous Institute under Kakatiya University, Warangal)

SEMESTER Vs COURSE CATEGORY WEIGHTAGE

(in terms of Total No. of Courses / Total No. Credits)

Semester	Number of Courses / Number of Credits (Course Category wise)								
	BSC	ESC	HSMC	PCC	OE	PE	PROJ	MC	TOTAL
I	3/9	4/12	-	-	-	-	-	2/0	9/21
II	3/9	5/10	1/3	-	-	-	-	1/0	10/22
III	1/4	1/2	1/1	4/10	2/4	-	-	-	9/21
IV	-	-	1/1	7/17	1/4	-	-	2/0	11/22
V	-			7/15	-	1/3	1/1	1/0	10/19
VI	-	1/3	2/4	5/11	-	1/3	1/1	-	10/22
VII	-	-	-	3/5	1/3	2/6	1/3	1/0	8/17
VIII	-	-	-	-	1/3	2/6	1/7	-	4/16
Total	7/22	11/27	5/9	26/58	5/14	6/18	4/12	7/0	71/160
% Weightage of Course Category	13.75 % (22/160)	16.87 % (27/160)	5.625 % (9/160)	36.25 % (58/160)	8.75 % (14/160)	11.25 % (18/160)	7.5 % (12/160)	0 %	100 % (160/160)
* Considering UHV. If course to be offered in future.									

* Considering UHV- II course to be offered in V semester as Mandatory course (MC) with zero credits (Not as HSMC course with 3 credits as suggested by AICTE)

W. Venkateshwar Reddy
Dr.V.Venkateshwar Reddy,
Assoc. Professor

S.P. Girija
S.P.Girija,
Assoc. Professor

Dr. M.Raju
Dr. M.Raju,
Assoc. Professor

Dr. G. Raghobham Reddy
Dr. G. Raghobham Reddy, Professor

Smt. A. Vijaya
Smt. A. Vijaya,
Assoc. Professor

Prof. K. Ashoka Reddy
Prof. K. Ashoka Reddy,
Principal

E. Suresh
E. Suresh,
Assoc. Professor or

Dr. B. Rama Devi
Dr.B.RamaDevi, Professor &
Head, Chairperson-BoS in ECE